ZARLINK SEMICONDUCTOR™

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Features

- Provides T1 clock at 1.544 MHz locked to input frame pulse
- Sources CEPT (30+2) Digital Trunk/ST-BUS clock and timing signals locked to internal or external 8 kHz signal
- TTL compatible logic inputs and outputs
- Uncommitted 2-input NAND gate
- Single 5 volt power supply
- Low power ISO-CMOS technology

Applications

- Synchronization and timing control for T1 and CEPT digital trunk transmission links
- ST- BUS clock and frame pulse source

Ordering Information

MT8940AE 24 Pin Plastic DIP (600 mil)

-40°C to +85°C

Description

The MT8940 is a dual digital phase-locked loop providing the timing and synchronization signals for the T1 or CEPT transmission links and the ST-BUS. The first PLL provides the T1 clock (1.544 MHz) synchronized to the input frame pulse at 8 kHz. The timing signals for the CEPT transmission link and the ST-BUS are provided by the second PLL locked to an internal or an external 8 kHz frame pulse signal.

The MT8940 is fabricated in Zarlink's ISO-CMOS technology.

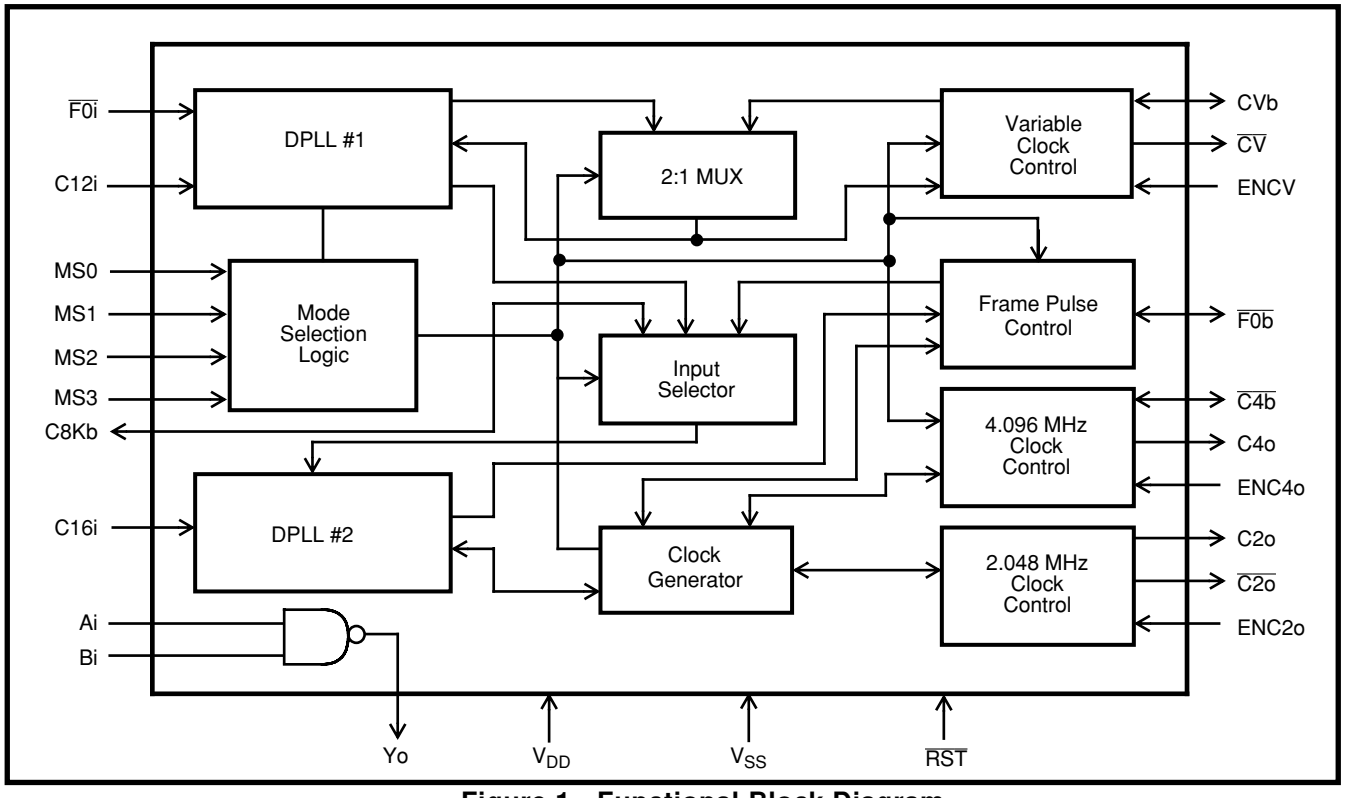

Figure 1 - Functional Block Diagram

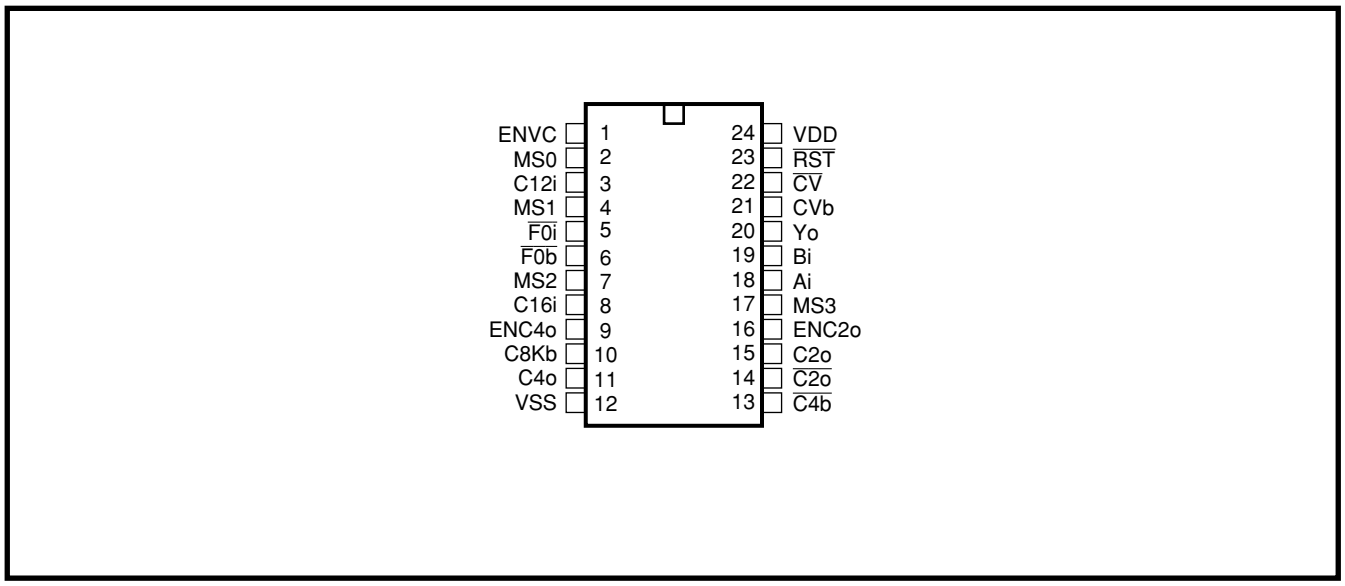

Figure 2 - Pin Connections

Pin Description

Pin #	Name	Description
1	EN_{CV}	**Variable clock enable (TTL compatible input)** - This input (pulled internally to V_{DD}) directly controls the three states of $\overline{CV}$ (pin 22) under all modes of operation. When HIGH, enables $\overline{CV}$ and when LOW, puts it in high impedance condition. It also controls the three states of CVb signal (pin 21) if MS1 is LOW. When EN_{CV} is HIGH, the pin CVb is an output and when LOW, it is in high impedance state. However, if MS1 is HIGH, CVb is always an input.
2	MS0	**Mode select '0' input (TTL compatible) -** This input (pulled internally to V_{SS}) in conjunction with MS1 (pin 4) selects the major mode of operation for both DPLLs. (Refer to Tables 1 and 2).
3	C12i	**Clock 12.355 MHz input (TTL compatible) -** Master clock input at 12.355 MHz ±100ppm for DPLL #1.
4	MS1	**Mode select-1 input (TTL compatible) -** This input (pulled internally to V_{SS}) in conjunction with MS0 (pin 2) selects the major mode of operation for both DPLLs. (Refer to Tables 1 and 2)
5	$\overline{F0i}$	**Frame pulse input (TTL compatible) -** This is the frame pulse input (pulled internally to V_{DD}) at 8 kHz. The DPLL #1 locks to the falling edge of this input to generate T1 (1.544 MHz) clock.
6	$\overline{F0b}$	**Frame pulse Bidirectional (TTL compatible input and Totem-pole output) -** Depending on the minor mode selected for the DPLL #2, it provides the 8 kHz frame pulse output or acts as an input (pulled internally to V_{DD}) to an external frame pulse.
7	MS2	**Mode select-2 input (TTL compatible) -** This input (pulled internally to V_{DD}) in conjunction with MS3 (pin 17) selects the minor mode of operation for the DPLL #2. (Refer to Table 3.)
8	C16i	**Clock 16.388 MHz input (TTL compatible) -** Master clock input at 16.388 MHz±32 ppm for DPLL #2.
9	EN_{C4o}	**Enable 4.096 MHz clock (TTL compatible input)** - This active high input (pulled internally to V_{DD}) enables C4o (pin 11) output. When LOW, the output C4o is in high impedance condition.

Pin Description (continued)

Pin #	Name	Description
10	C8Kb	**Clock 8 kHz- Bidirectional (TTL compatible input and open drain output with 100K internal resistor to V_{DD})** - This is the 8 kHz input signal on the rising edge of which DPLL #2 locks during its NORMAL mode. When DPLL #2 is in SINGLE CLOCK mode, this pin outputs an 8 kHz signal provided by DPLL #1, which is also connected internally to DPLL #2.
11	C4o	**Clock 4.096 MHz (Three state output) -** This is the inverse of the signal appearing on pin 13 ($\overline{C4b}$) at 4.096 MHz and has a rising edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C4o} (pin 9).
12	V_{SS}	**Ground (0 Volt)**
13	$\overline{C4b}$	**Clock 4.096 MHz- Bidirectional (TTL compatible input and Totem-pole output)** - When the mode select bit MS3 (pin 17) is HIGH, it provides the 4.096 MHz clock output with the falling edge in the frame pulse ($\overline{F0b}$) window. When pin 17 is LOW, $\overline{C4b}$ is an input (pulled internally to V_{DD}) to an external clock at 4.096 MHz.
14	$\overline{C2o}$	**Clock 2.048 MHz (Three state output)** - This is the divide by two output of $\overline{C4b}$ (pin 13) and has a falling edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C2o} (pin 16).
15	C2o	**Clock 2.048 MHz (Three state output) -** This is the divide by two output of $\overline{C4b}$ (pin 13) and has a rising edge in the frame pulse ($\overline{F0b}$) window. The high impedance state of this output is controlled by EN_{C2o} (pin 16).
16	EN_{C2o}	**Enable 2.048 MHz clock (TTL compatible input)** - This active high input (pulled internally to V_{DD}) enables both $\overline{C2o}$ and C2o outputs (pins 14 and 15). When LOW, these outputs are in high impedance condition.
17	MS3	**Mode select 3 input (TTL compatible) -** This input (pulled internally to V_{DD}) in conjunction with MS2 (pin 7) selects the minor mode of operation for DPLL #2. (Refer to Table 3.)
18,19	Ai, Bi	**Inputs A and B (TTL compatible) -**These are the two inputs (pulled internally to V_{SS}) of the uncommitted NAND gate.
20	Y_o	**Output Y (Totem pole output) -** Output of the uncommitted NAND gate.
21	CVb	**Variable clock Bidirectional (TTL compatible input and Totem-pole output) -** When acting as an output (MS1-LOW) during the NORMAL mode of DPLL #1, this pin provides the 1.544 MHz clock locked to the input frame pulse $\overline{F0i}$ (pin 5). When MS1 is HIGH, it is an input (pulled internally to V_{DD}) to an external clock at 1.544 MHz or 2.048 MHz to provide the internal signal at 8 kHz to DPLL #2.
22	$\overline{CV}$	**Variable clock (Three state output) -** This is the inverse output of the signal appearing on pin 21, the high impedance state of which is controlled EN_{CV} (pin 1).
23	$\overline{RST}$	**Reset (Schmitt trigger input) -**This input (active LOW) evokes reset condition for the device.
24	V_{DD}	**V_{DD} (+5V)** Power supply.

Functional Description

The MT8940 is a dual digital phase-locked loop providing the timing and synchronization signals to the interface circuits for T1 and CEPT (30+2) Primary Multiplex Digital Transmission links. As shown in Figure 1, it has two digital phase-locked loops (DPLLs), associated output controls and the mode selection logic circuits. The two DPLLs, although similar in principle, operate independently to provide T1 (1.544 MHz) and CEPT (2.048 MHz) transmission clocks, and ST-BUS timing signals.

The principle of operation behind the two DPLLs is shown in Figure 3. A master clock is divided down to 8 kHz where it is compared with the 8 kHz input, and depending on the output of the phase comparison, the master clock frequency is corrected. The MT8940 achieves the frequency correction in both directions by using the master clock at a slightly higher frequency and dividing it unaltered or stretching its period (at two discrete instants in a frame) before the division depending on the phase comparison output. When the input frequency is

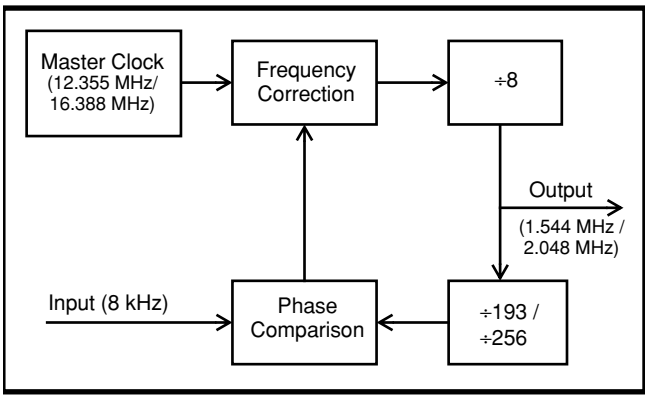

Figure 3 - DPLL Principle

higher, the unchanged master clock is divided, thus effectively speeding-up the locally generated clock and eventually pulling it in synchronization with the input. If the input frequency is lower than the divided master clock, the period of the master clock is stretched by half a cycle, at two discrete instants in a phase sampling period. This introduces a total delay of one master clock period over the sampling duration, which is then divided to generate the local signal synchronous with the input. Once the output is phase-locked to the active edge of the input, the circuit will maintain the locked condition as long as the input frequency is within the lock-in range (±1.04 Hz) of the DPLLs. The lock-in range is wide enough to meet the CCITT line rate specification (1.544 MHz±130ppm and 2.048 MHz ±50ppm) for the High Capacity Terrestrial Digital Service.

The phase sampling is done once in a frame (8 kHz) and the divisions are set at 8 and 193 for DPLL #1, which locks on to the falling edge of the input at 8 kHz to generate T1 (1.544 MHz) clock. Although the phase sampling duration is the same for DPLL #2, the divisions are set at 8 and 256 to provide the CEPT/ST-BUS clock at 2.048 MHz synchronized to the rising edge of the input signal (8 kHz). The master clock source is specified to be at 12.355 MHz ±100 ppm for DPLL #1 and 16.388 MHz ±32 ppm for DPLL #2 over the entire temperature range of operation.

The inputs MS0 to MS3 are used to select the operating mode of the MT8940, see Tables 1 to 4. All the outputs are individually controlled to the high impedance condition by their respective enable controls. The uncommitted NAND gate is available for use in applications involving Zarlink's MT8976/MH89760 (T1 interfaces) and MT8979/MH89790 (CEPT interfaces).

Modes of Operation

The operation of the MT8940 is categorized into major and minor modes. The major modes are defined for both DPLLs by the mode select pins MS0 and MS1. The minor modes are selected by MS2 and MS3, and are applicable only to DPLL #2. There are no minor modes for DPLL #1.

Major modes of the DPLL #1

DPLL #1 can be operated in three major modes as selected by MS0 and MS1 (Table 1). When MS1 is LOW, it is in NORMAL mode, which provides a T1 (1.544 MHz) clock signal locked to the falling edge of the input frame pulse $\overline{F0i}$ (8 kHz). DPLL#1 requires a master clock input of 12.355 MHz±100 ppm (C12i). In the second and third major modes (MS1 is HIGH), DPLL #1 is set to DIVIDE an external 1.544 MHz or 2.048 MHz signal applied at CVb (pin 21). The division can be set by MS0 to be either 193 (LOW) or 256 (HIGH). In these modes, the 8 kHz output is connected internally to DPLL #2, which operates in SINGLE CLOCK mode.

Major modes of the DPLL #2

There are four major modes for DPLL #2 selectable by MS0 and MS1, as shown in Table 2. In all these modes DPLL #2 provides the CEPT PCM 30 timing, and the ST-BUS clock and framing signals.

In NORMAL mode, DPLL #2 provides the CEPT and ST-BUS compatible timing signals locked to the rising edge of the 8 kHz input signal (C8Kb). These

signals are the 4.096 MHz (C4o and $\overline{C4b}$) and the 2.048 MHz (C2o and $\overline{C2o}$) clocks, and the 8 kHz

MS0	MS1	Mode of operation	Function
X	0	NORMAL	Provides the T1 (1.544 MHz) clock synchronized to the falling edge of the input frame pulse ($\overline{F0i}$).
0	1	DIVIDE-1	DPLL #1 divides the CVb input by 193. The divided output is connected to DPLL #2.
1	1	DIVIDE-2	DPLL #1 divides the CVb input by 256. The divided output is connected to DPLL #2.

Note: X: indicates don't care

Table 1. Major Modes of the DPLL #1

frame pulse ($\overline{F0b}$), which are derived from the 16.388 MHz master clock. This mode can also provide the ST-BUS timing and framing signals with the input (C8Kb) tied HIGH and the master clock set at 16.384 MHz. The DPLL makes no correction in this configuration and provides the timing signals compatible to the ST-BUS format without any jitter.

In FREE-RUN mode, DPLL #2 generates CEPT and ST-BUS timing and framing signals with no external inputs except the master clock set at 16.388 MHz. Since the master clock source is set at a higher frequency than the nominal value, the DPLL makes the necessary corrections to deliver the averaged timing signals compatible to the ST-BUS format.

The operation of DPLL #2 in SINGLE CLOCK-1 mode is identical to SINGLE CLOCK-2 mode, providing the CEPT and ST-BUS compatible timing signals synchronized to the internal 8 kHz signal obtained from DPLL#1 in DIVIDE mode. When SINGLE CLOCK-1 mode is selected for DPLL #2, it automatically selects the DIVIDE-1 mode for DPLL #1, and thus, an external 1.544 MHz clock signal applied at CVb (pin 21) is divided by DPLL #1 to generate the internal signal at 8 kHz onto which DPLL #2 locks. Similarly when SINGLE CLOCK-2 mode is selected, DPLL #1 is in DIVIDE-2 mode, with an external signal of 2.048 MHz providing the internal 8 kHz signal to DPLL #2. In both these modes, this internal signal is available on C8Kb (pin 10) and DPLL #2 locks to its falling edge to provide the CEPT and ST-BUS compatible timing signals. This is in contrast to the Normal mode where these timing signals are synchronized with the rising edge of the 8 kHz signal on C8Kb.

Minor modes of the DPLL #2

The minor modes for DPLL #2 depends upon the status of the mode select bits MS2 and MS3 (pins 7 and 17).

MS0	MS1	Mode of operation	Function
0	0	NORMAL	Provides ST-BUS/CEPT timing signals locked to the rising edge of the 8kHz input signal at C8Kb.
1	0	FREE-RUN	Provides ST-BUS timing and framing signals with no external inputs, except the master clock.
0	1	SINGLE CLOCK-1	Provides the CEPT/ST-BUS compatible timing signals locked to the falling edge of the 8kHz internal signal provided by DPLL #1.
1	1	SINGLE CLOCK-2	Provides CEPT/ST-BUS timing signals locked to the falling edge of the 8kHz internal signal provided by DPLL #1.

Table 2. Major Modes of the DPLL #2

When MS3 is HIGH, DPLL #2 operates in any of the major modes as selected by MS0 and MS1.

When MS3 is LOW, it overrides the major mode selected and DPLL #2 accepts an external clock of 4.096 MHz on $\overline{C4b}$ (pin 13) to provide the 2.048 MHz clocks (C2o and $\overline{C2o}$) and the 8 kHz frame pulse ($\overline{F0b}$) compatible with the ST-BUS format.

The mode select bit MS2, controls the signal direction of $\overline{F0b}$ (pin 6). When MS2 is LOW, $\overline{F0b}$ is an input for an external frame pulse at 8 kHz. This

MS2	MS3	Functional Description
1	1	Provides ST-BUS 4.096 MHz and 2.048 MHz clocks and 8kHz frame pulse depending on the major mode selected.
0	1	Provides ST-BUS 4.096 MHz & 2.048 MHz clocks depending on the major mode selected while $\overline{F0b}$ acts as an input. However, the input on $\overline{F0b}$ has no effect on the operation of DPLL #2 unless it is in FREE-RUN mode.
0	0	Overrides the major mode selected and accepts properly phase related external 4.096 MHz clock and 8 kHz frame pulse to provide the ST-BUS compatible clock at 2.048MHz.
1	0	Overrides the major mode selected and accepts a 4.096 MHz external clock to provide the ST-BUS clock and frame pulse at 2.048 MHz and 8 kHz, respectively.

Table 3. Minor Modes of the DPLL #2

input is effective only if MS3 is also LOW and $\overline{C4b}$ is accepting a 4.096 MHz external clock, which has a proper phase relationship with the external input on $\overline{F0b}$ (refer to Figure 15). Otherwise, the input on pin

$\overline{F0b}$ will have no bearing on the operation of DPLL #2, unless it is in FREE-RUN mode as selected by MS0 and MS1. In FREE-RUN mode, the input on $\overline{F0b}$ is treated the same way as the C8Kb input in NORMAL mode. The frequency of the input signal on $\overline{F0b}$ should be 16 kHz for DPLL #2 to provide the ST-BUS compatible clocks at 4.096 MHz and 2.048 MHz.

When MS2 is HIGH, the $\overline{F0b}$ pin provides the ST-BUS frame pulse output locked to the 8kHz internal or external signal as determined by the other mode select pins MS0, MS1 and MS3.

Table 4 summarizes the modes of the two DPLLs. It should be noted that each of the major modes selected for DPLL #2 can have any of the minor modes, although some of the combinations are functionally similar. The required operation of both DPLL#1 and DPLL#2 must be considered when determining MS0-MS3.

MODE #	MS 0	MS 1	MS 2	MS 3	Operating Modes	
					DPLL #1	**DPLL #2**
0	0	0	0	0	NORMAL MODE	Properly phase related External 4.096 MHz clock and 8 kHz frame pulse provide the ST-BUS clock at 2.048 MHz.
1	0	0	0	1	NORMAL MODE	NORMAL MODE $\overline{F0b}$ is an input but has no function in this mode.
2	0	0	1	0	NORMAL MODE	External 4.096 MHz provides the ST-BUS clock and Frame Pulse at 2.048 MHz and 8 kHz, respectively.
3	0	0	1	1	NORMAL MODE: Provides the T1 (1.544 MHz) clock synchronized to the falling edge of the input frame pulse ($\overline{F0i}$).	NORMAL MODE: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz input signal (C8Kb).
4	0	1	0	0	DIVIDE-1 MODE	Same as mode '0'.
5	0	1	0	1	DIVIDE-1 MODE	SINGLE CLOCK-1 MODE $\overline{F0b}$ is an input, but has no function in this mode.
6	0	1	1	0	DIVIDE-1 MODE	Same as mode 2.
7	0	1	1	1	DIVIDE-1 MODE: Divides the CVb input by 193. The divided output is connected to DPLL #2.	SINGLE CLOCK-1 MODE: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz internal signal provided by DPLL #1.
8	1	0	0	0	NORMAL MODE	Same as mode '0'.
9	1	0	0	1	NORMAL MODE	$\overline{F0b}$ is an input and DPLL #2 locks on to it only if it is at 16 kHz to provide the ST-BUS control signals.
10	1	0	1	0	NORMAL MODE	Same as mode 2.
11	1	0	1	1	NORMAL MODE Provides the T1 (1.544 MHz) clock synchronized to the falling edge of input frame pulse ($\overline{F0i}$).	FREE-RUN MODE: Provides the ST-BUS timing signals with no external inputs except the master clock.
12	1	1	0	0	DIVIDE-2 MODE	Same as mode '0'.
13	1	1	0	1	DIVIDE-2 MODE	SINGLE CLOCK-2 MODE: $\overline{F0b}$ is an input, but has no function in this mode.
14	1	1	1	0	DIVIDE-2 MODE	Same as mode 2.
15	1	1	1	1	DIVIDE-2 MODE: Divides the CVb input by 256. The divided output is connected to DPLL#2.	SINGLE CLOCK-2 MODE: Provides the CEPT/ST-BUS compatible timing signals locked to the 8 kHz internal signal provided by DPLL #1.

Table 4. Summary of Modes of Operation - DPLL #1 and #2

Applications

The following figures illustrate how the MT8940 can be used in a minimum component count approach to providing the timing and synchronization signals for the Zarlink T1 and CEPT interfaces, and the ST-BUS. The hardware selectable modes and the independent control over each PLL adds flexibility to the interface circuits. It can be easily reconfigured to provide the timing and control signals for both at the master and slave ends of the link.

Synchronization and Timing Signals for the T1 Transmission Link

Figures 4 and 5 show examples of how to generate the timing signals for the master and slave ends of a T1 link.

At the master end of the link (Figure 4), DPLL #2 is the source of the ST-BUS signals derived from the 4.096 MHz system clock. The frame pulse output is looped back to DPLL #1 (in NORMAL mode), which locks to it to generate the T1 line clock. The timing relationship between the 1.544 MHz T1 clock and the 2.048 MHz ST-BUS clock meets the requirements of the MH89760/760B. The crystal clock at 12.355 MHz is used by DPLL #1 to generate the 1.544 MHz clock, while DPLL #2 uses the 4.096 MHz system clock to provide the ST-BUS timing signals. The ST-BUS signals can also be obtained from DPLL #2 in FREE-RUN mode, using a crystal clock at 16.388 MHz instead of 4.096 MHz system clock. The uncommitted NAND gate converts the received signals, RxA and RxB of the MH89760 to a single Return to Zero (RZ) input for the clock extraction circuits of the MH89760. This is not required for the MH89760B. The generated ST-BUS signals can be used to synchronize the system and the switching equipment at the master end.

At the slave end of the link (Figure 5) both the DPLLs are in NORMAL mode with DPLL #2 providing the ST-BUS timing signals locked to the 8 kHz frame pulse (E8Ko) extracted from the received signal on the T1 line. The regenerated frame pulse is looped back to DPLL #1 to provide the T1 line clock as at the master end. The 12.355 MHz and 16.388 MHz crystal clock sources are necessary for DPLL #1 and #2.

Synchronization and Timing Signals for the CEPT Transmission Link

The MT8940 can be used to provide the timing and synchronization signals for the MH89790/790B, Zarlink's CEPT(30+2) digital trunk interface hybrid. Since the operational frequencies of the ST-BUS and the CEPT primary multiplex digital trunk are same, only DPLL #2 is required to achieve synchronization between the two.

Figures 6 and 7 show how the MT8940 can be used to synchronize the ST-BUS and the CEPT transmission link at the master and slave ends, respectively.

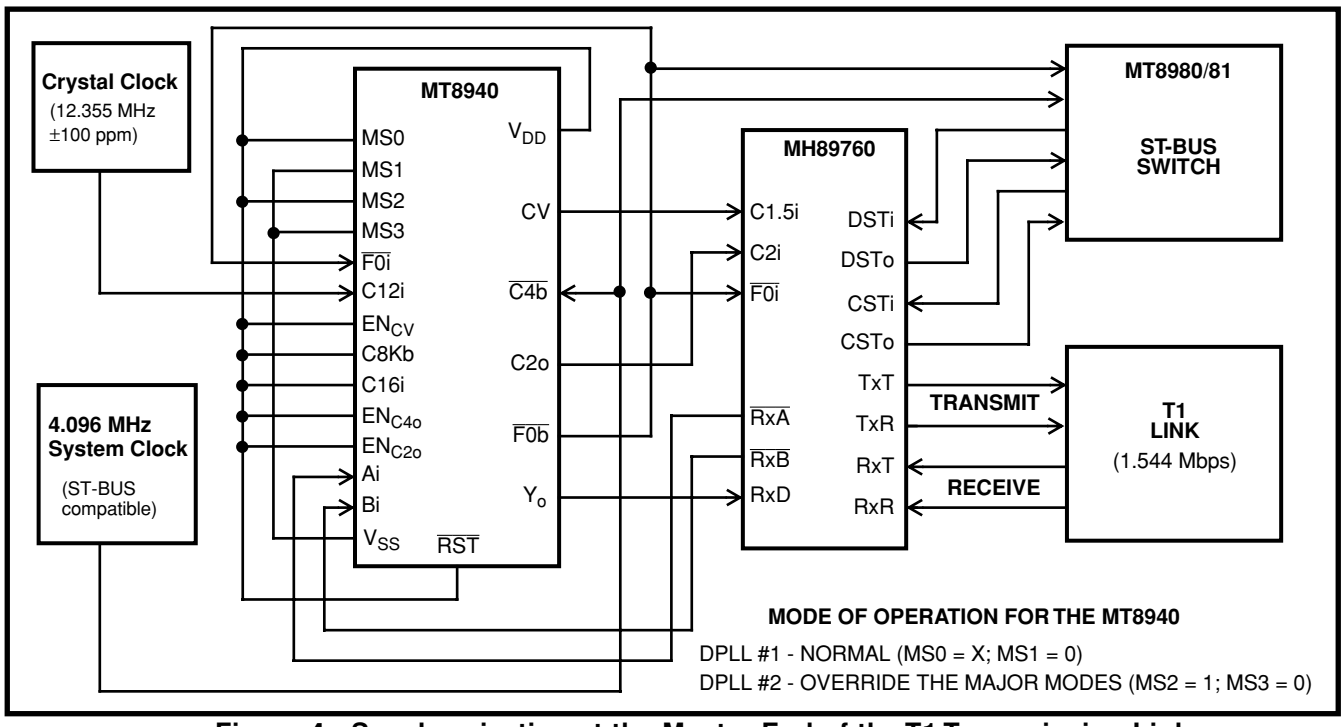

Figure 4 - Synchronization at the Master End of the T1 Transmission Link

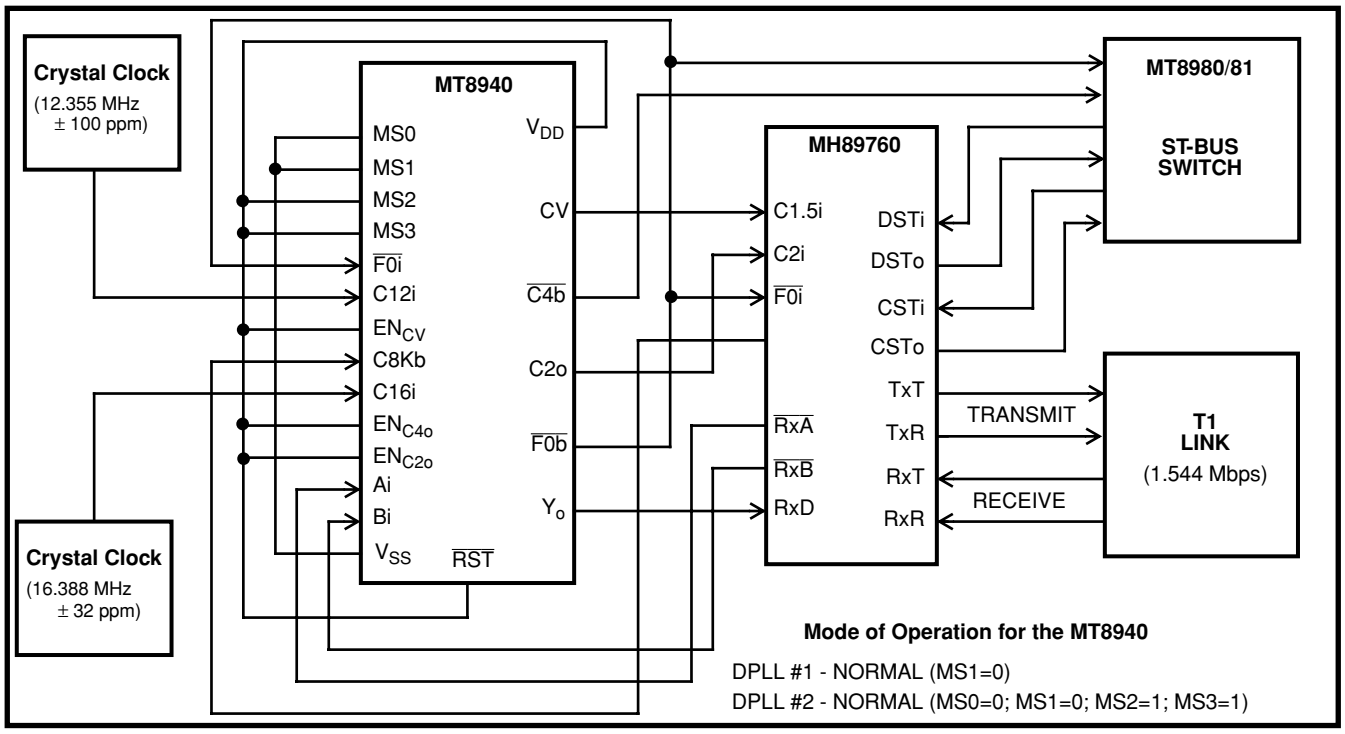

Figure 5 - Synchronization at the Slave End of the T1 Transmission Link

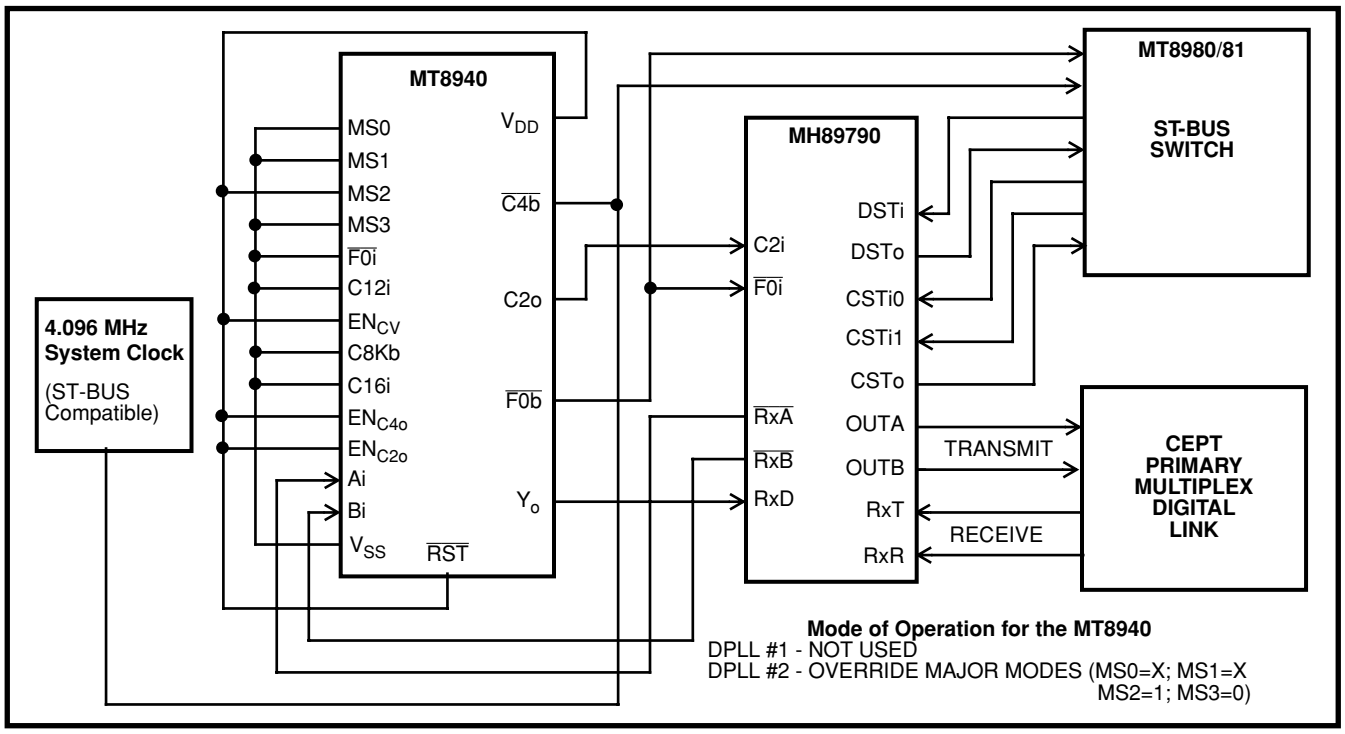

Figure 6 - Synchronization at the Master End of the CEPT Digital Transmission Link

Generation of ST-BUS Timing Signals

The MT8940 can source the properly formatted ST-BUS timing and control signals with no external inputs except the crystal clock. This can be used as the standard timing source for ST-BUS systems or any other system with similar clock requirements. Figure 8 shows two such applications using only DPLL #2. In one case, the MT8940 is in FREE-RUN mode with an oscillator input of 16.388 MHz. This forces the DPLL to correct at a rate of 4 kHz to maintain the ST-BUS clocks, which therefore, will be jittered. In the other case, the oscillator input is 16.384 MHz (exactly eight times the output frequency) and DPLL #2 operates in NORMAL mode with C8Kb input tied HIGH. Since no corrections are necessary, the output is free from jitter. DPLL #1 is completely free in both cases and available for any other purpose.

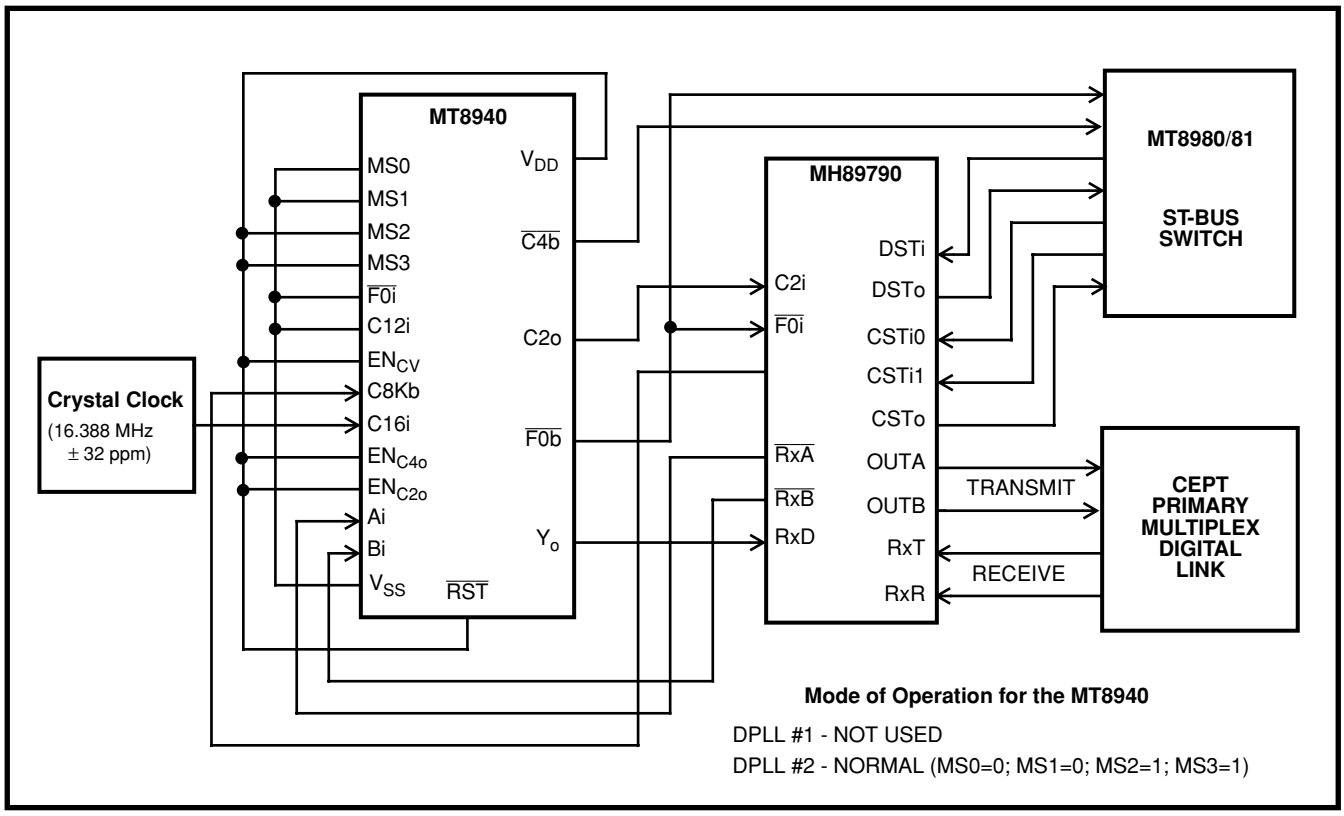

Figure 7 - Synchronization at the Slave End of the CEPT Digital Transmission Link

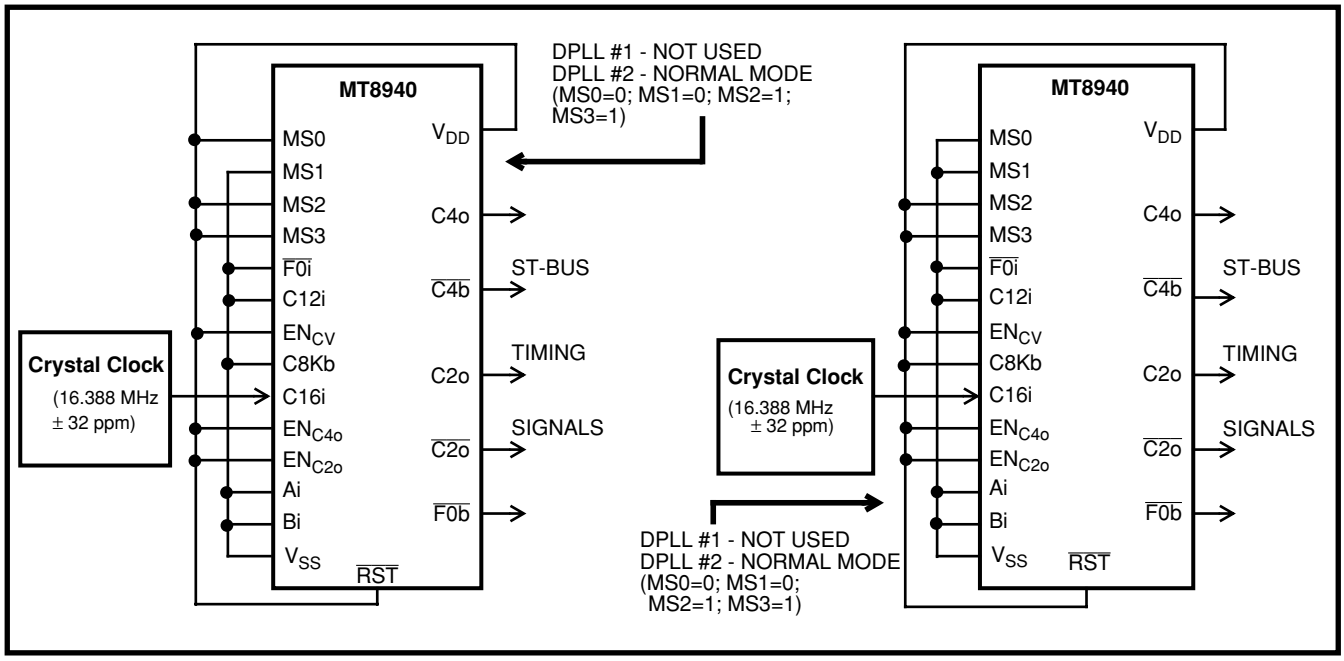

Figure 8 - Generation of the ST-BUS Timing Signals

Absolute Maximum Ratings*

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Symbol	Min	Max	Units
1	Supply Voltage	V_{DD}	-0.3	7.0	V
2	Voltage on any pin	V_I	V_{SS}-0.5	V_{DD}+0.5	V
3	Input/Output Diode Current	$I_{IK/OK}$		±10	mA
4	Output Source or Sink Current	I_O		±25	mA
5	DC Supply or Ground Current	I_{DD}/I_{SS}		±50	mA
6	Storage Temperature	T_{ST}	-65	150	°C
7	Package Power Dissipation LCC	P_D		600	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Input HIGH Voltage	V_{IH}	2.4		V_{DD}	V	For 400 mV noise margin
3	Input LOW Voltage	V_{IL}	V_{SS}		0.4	V	For 400 mV noise margin
4	Operating Temperature	T_A	-40	25	85	°C	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics

- Voltages are with respect to ground (V_{SS}) unless otherwise stated.

V_{DD}=5.0 V±5%; V_{SS}=0V; T_A=-40 to 85°C.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Supply Current	I_{DD} I_{DDS}		8	15 100	mA	Under clocked condition, with the inputs tied to the same supply rail as the corresponding pull-up / down resistors.
2	IN	Input HIGH voltage (For all the inputs except pin 23)	V_{IH}	2.0			V	
3	IN	Positive-going threshold voltage (For pin 23)	V_+	2.8			V	
4	IN	Input LOW voltage (For all the inputs except pin 23)	V_{IL}			0.8	V	
5	IN	Negative-going threshold voltage (For pin 23)	V_-			1.5	V	
6	OUT	Output current HIGH (For all the outputs except pin 10)	I_{OH}	-9.5			mA	V_{OH}=2.4 V
7	OUT	Output current LOW (For all the outputs except pin 10)	I_{OL}	4.5			mA	V_{OL}=0.4 V
8	OUT	Output current LOW (pin 10)	I_{OL}	2.0			mA	V_{OL}=0.4 V
9		Leakage current on bidirectional pins and all inputs except C12i, C16i, $\overline{RST}$	$I_{IZ/OZ}$			±150	µA	$V_{I/O}$=V_{SS} or V_{DD}
10		Leakage current on all outputs and C12i, C16i, $\overline{RST}$ inputs	$I_{IZ/OZ}$		±1	±10	µA	$V_{I/O}$=V_{SS} or V_{DD}

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figure 9)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DPLL #1	Frame pulse input ($\overline{F0i}$) to CVb output (1.544 MHz) delay	t_{F15H}	-40		75	ns	
2		CVb output (1.544 MHz) rise time	$t_{r1.5}$		10	15	ns	Test load circuit 1 (Fig. 17).
3		CVb output (1.544 MHz) fall time	$t_{f1.5}$		12	15	ns	Test load circuit 1 (Fig. 17).
4		CVb output (1.544 MHz) clock period	t_{P15}	648		690	ns	
5		CVb output (1.544 MHz) clock width (HIGH)	t_{W15H}	320		386	ns	
6		CVb output (1.544 MHz) clock width (LOW)	t_{W15L}	314		327	ns	
7		$\overline{CV}$ delay (HIGH to LOW)	t_{15HL}		5	30	ns	
8		$\overline{CV}$ delay (LOW to HIGH)	t_{15LH}		-12	10	ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

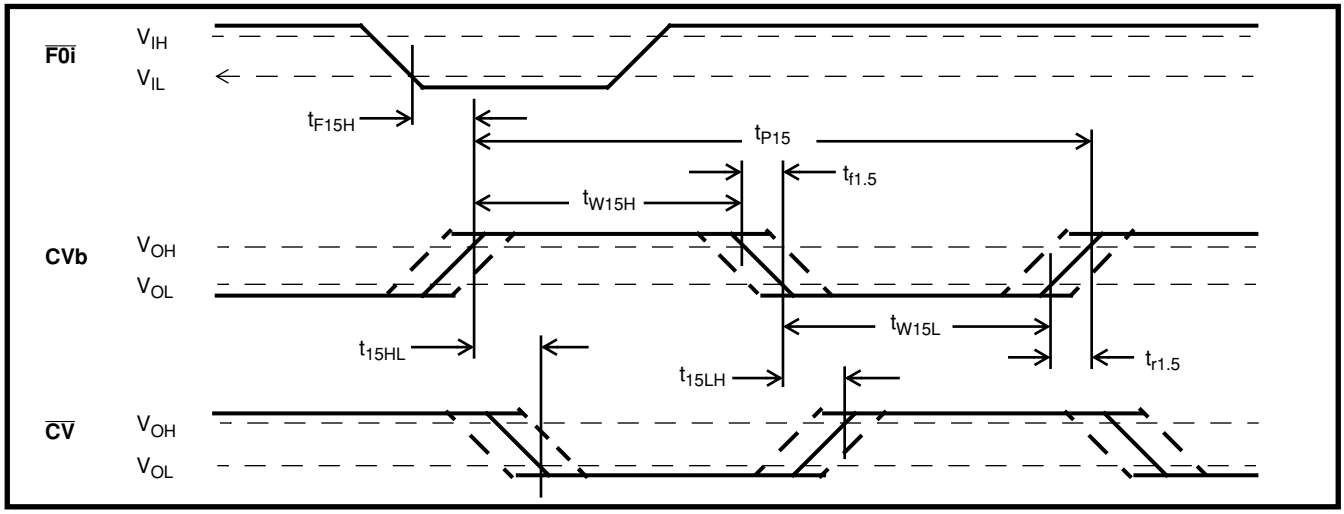

Figure 9 - Timing Information for DPLL #1 in NORMAL Mode

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figure 10)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DPLL #1	C8Kb output (8kHz) delay (HIGH to HIGH)	t_{C8HH}			130	ns	Test load circuit 2 (Fig. 17).
2		C8Kb output (8 kHz) delay (LOW to LOW)	t_{C8LL}		50	130	ns	Test load circuit 2 (Fig. 17).
3		C8Kb output duty cycle			66 50		% %	In Divide -1 Mode In Divide - 2 Mode
4		Inverted clock output delay (HIGH to LOW)	t_{ICHL}		40	75	ns	
5		Inverted clock output delay (LOW to HIGH)	t_{ICLH}		35	60	ns	

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‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

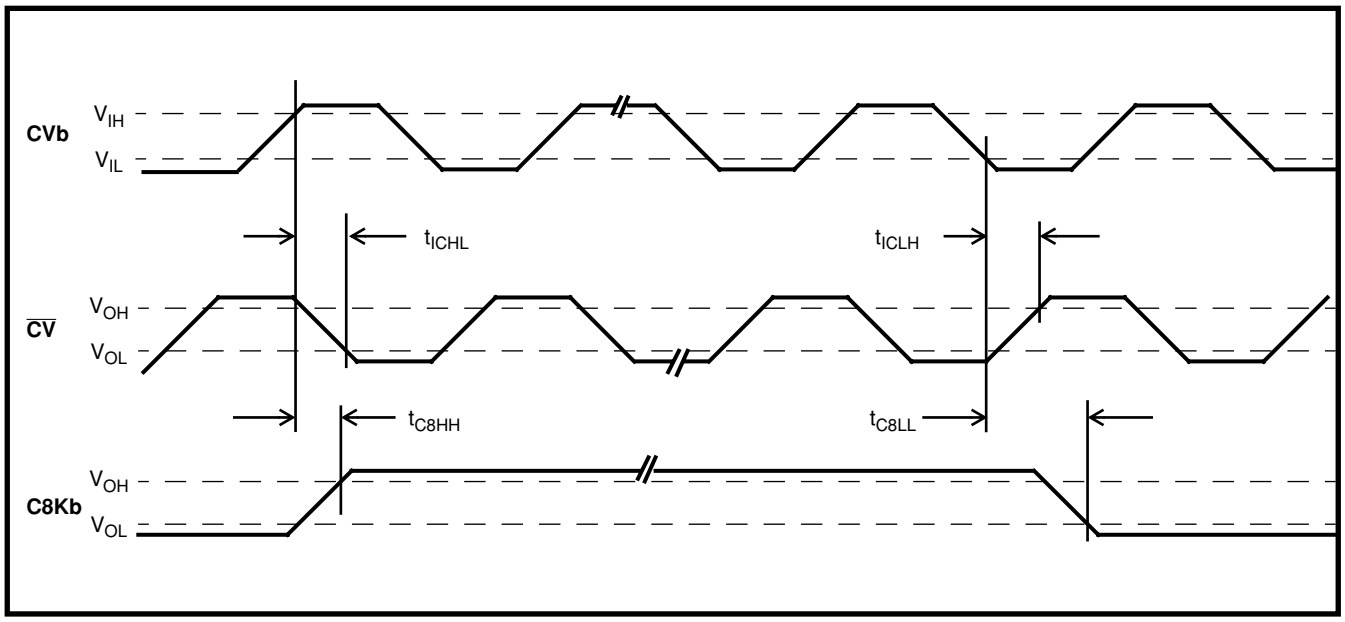

Figure 10 - DPLL #1 in DIVIDE Mode

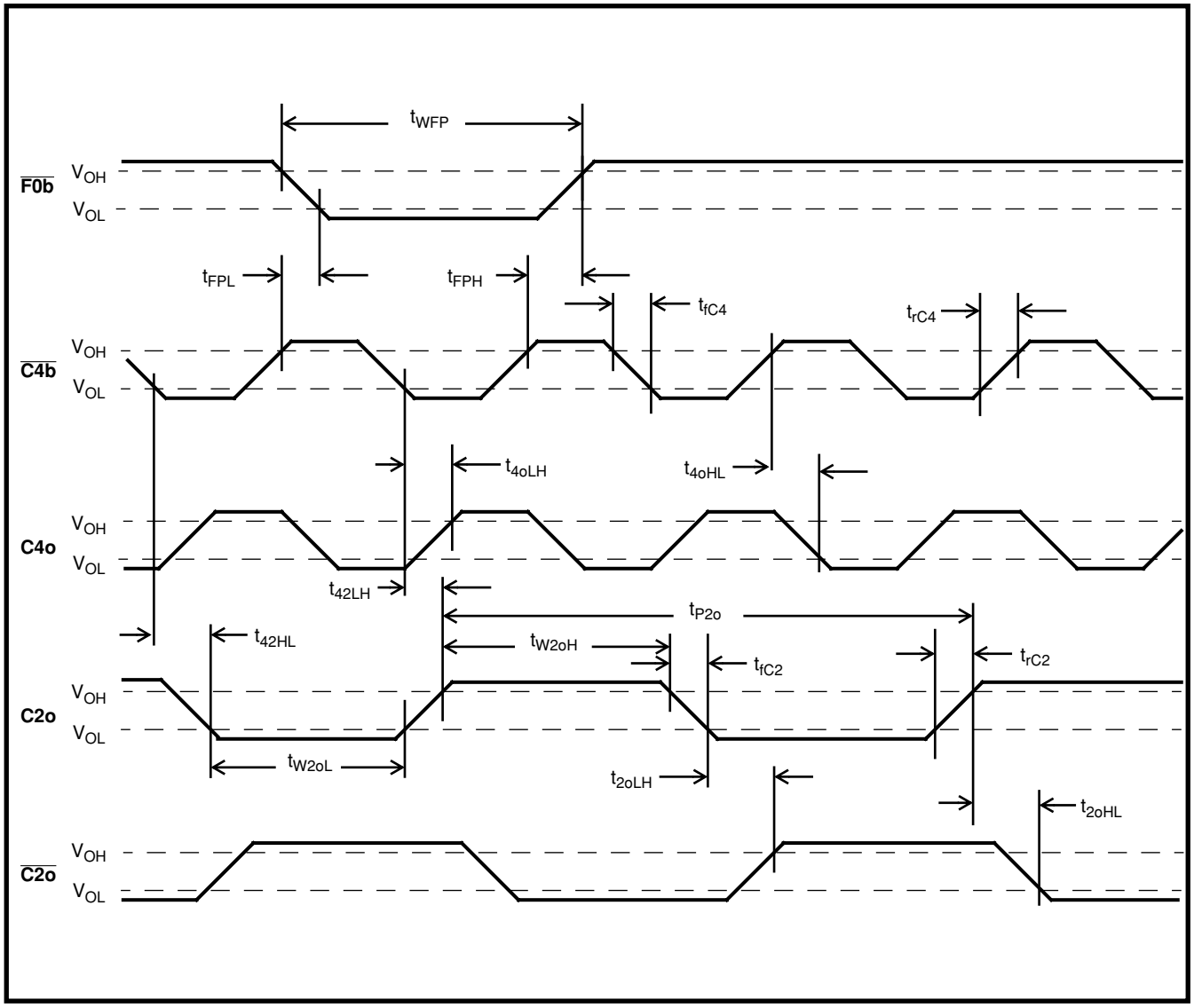

Figure 11 - Timing Information on DPLL #2 Outputs

AC Electrical Characteristics† -Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figures 11&12)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DPLL #2	$\overline{C4b}$ output delay (HIGH to LOW) from C8Kb input/output	t_{84H}	-25		75	ns	Test load circuit 2 (Fig. 17) on C8Kb.
2		$\overline{C4b}$ output clock period	t_{P4o}	240		282	ns	Test load circuit 1 (Fig. 17).
3		$\overline{C4b}$ output clock width (HIGH)	t_{W4oH}	123		165	ns	
4		$\overline{C4b}$ output clock width (LOW)	t_{W4oL}	110		123	ns	
5		$\overline{C4b}$ output clock rise time	t_{rC4}			10	ns	Test load circuit 1 (Fig. 17).
6		$\overline{C4b}$ clock output fall time	t_{fC4}			10	ns	Test load circuit 1 (Fig. 17).
7		Frame pulse output delay (HIGH to LOW) from $\overline{C4b}$	t_{FPL}			50	ns	Test load circuit 1 (Fig. 17).
8		Frame pulse output delay (LOW to HIGH) from $\overline{C4b}$	t_{FPH}			40	ns	Test load circuit 1 (Fig. 17).
9		Frame pulse ($\overline{F0b}$) width	t_{WFP}	200		245	ns	
10		C4o delay - LOW to HIGH	t_{4oLH}			45	ns	
11		C4o delay - HIGH to LOW	t_{4oHL}			45	ns	
12		$\overline{C4b}$ to C2o delay (LOW to HIGH)	t_{42LH}	-10		+10	ns	
13		$\overline{C4b}$ to C2o delay (HIGH to LOW)	t_{42HL}			20	ns	
14		C2o clock period	t_{P2o}	486		523	ns	Test load circuit 1 (Fig. 10).
15		C2o clock width (HIGH)	t_{W2oH}	244		291	ns	
16		C2o clock width (LOW)	t_{W2oL}	233		244	ns	
17		C2o clock rise time	t_{rC2}			10	ns	Test load circuit 1 (Fig. 10).
18		C2o clock fall time	t_{fC2}			10	ns	Test load circuit 1 (Fig. 10).
19		$\overline{C2o}$ delay - LOW to HIGH	t_{2oLH}			20	ns	
20		$\overline{C2o}$ delay - HIGH to LOW	t_{2oHL}	-5		30	ns	

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‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

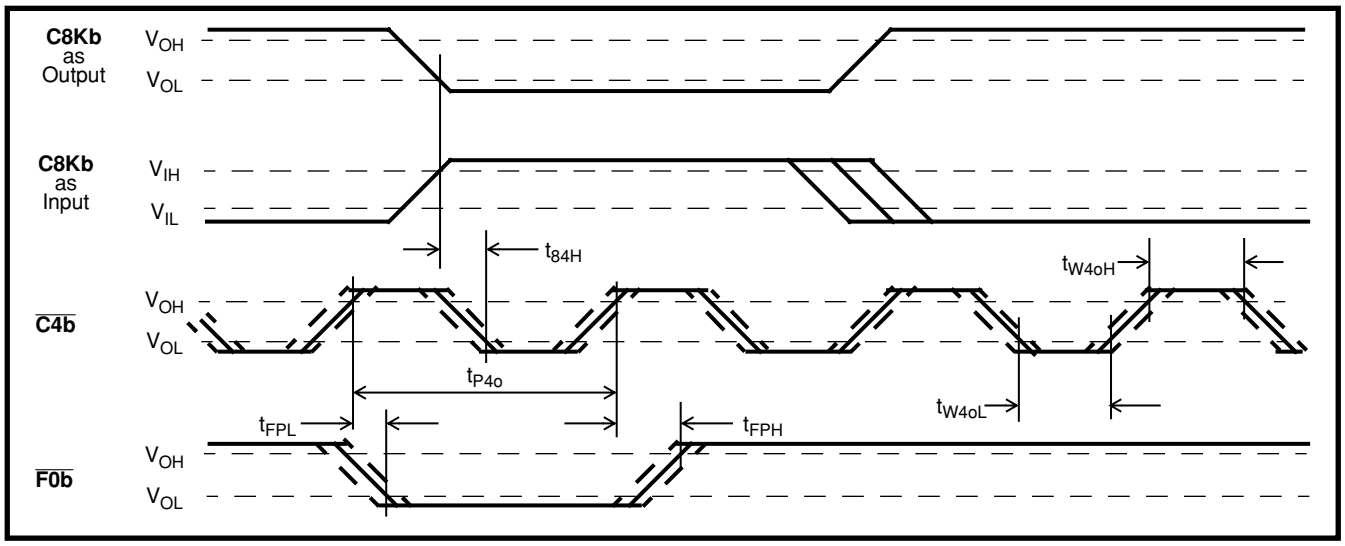


Figure 12 - ST-BUS Timings from DPLL #2 and C8Kb Input/Output

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. (Ref. Figure 13)

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\overline{CV}$/CVb (1.544 MHz) Setup time	t_{S15}	25			ns	
2	$\overline{CV}$/CVb (1.544 MHz) Hold time	t_{H15}	110			ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

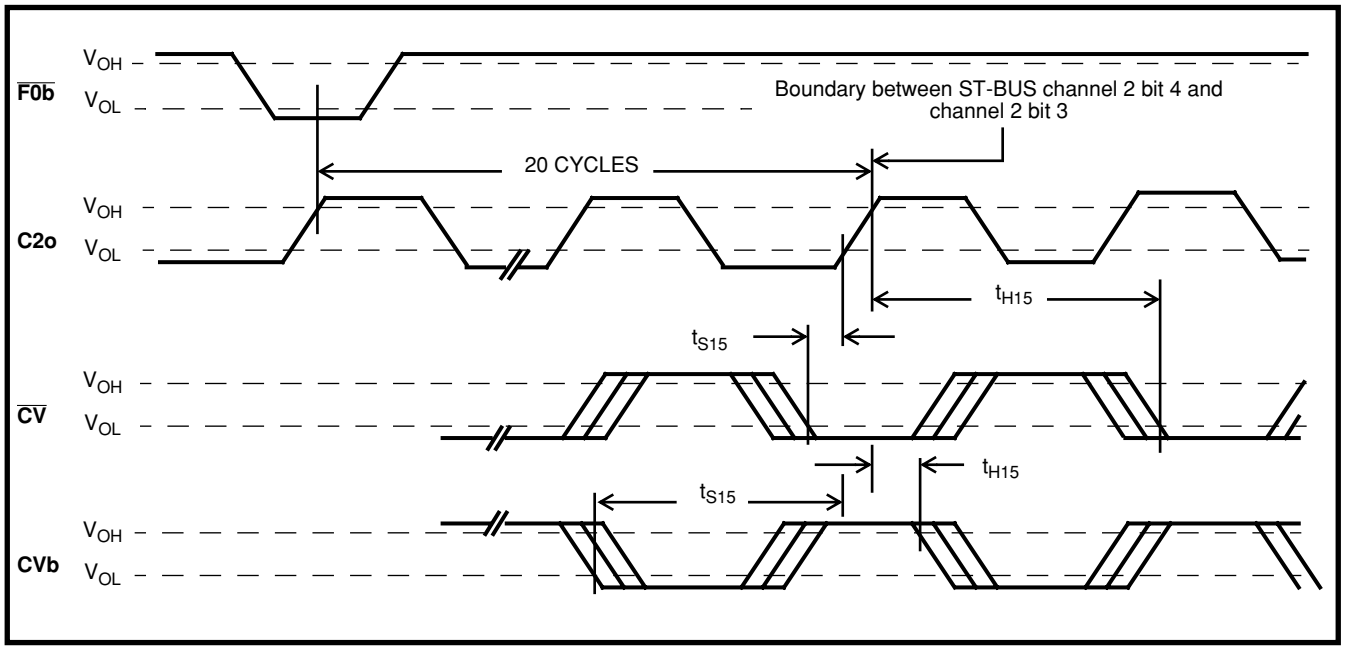


Figure 13 - $\overline{F0b}$ from DPLL #2 is Looped Back as Input to DPLL #1 (T1 Line synchronized to ST-BUS)

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figure 14)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	CLOCKS	Master clocks input rise time	t_r			10	ns	
2		Master clocks input fall time	t_f			10	ns	
3		Master clock period (12.355MHz)	t_{P12}	80.930	80.938	80.946	ns	For DPLL #1, while operating to provide the T1 clock signal.
4		Master clock period (16.388MHz)	t_{P16}	61.018	61.020	61.022	ns	For DPLL #2, while operating to provide the CEPT and ST-BUS timing signals.
5		Duty Cycle of master clocks		45	50	55	%	
6		Lock-in Range (For each PLL)		-1.5		+1.04	Hz	With the Master clocks as shown above.

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

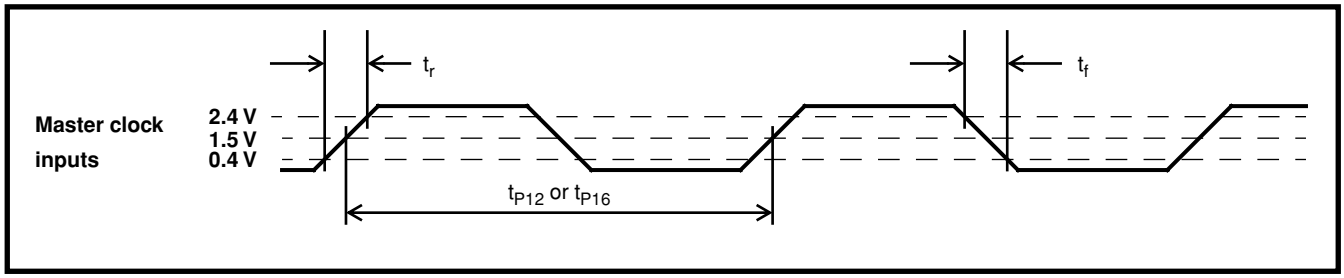


Figure 14 - Master Clock Inputs

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figure 15)**

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	$\overline{F0b}$ input pulse width (LOW)	t_{WFP}	40			ns	
2	$\overline{C4b}$ input clock period	t_{P4o}	.080		50	µs	
3	Frame pulse ($\overline{F0b}$) setup time	t_{FS}	25			ns	
4	Frame pulse ($\overline{F0b}$) hold time	t_{FH}	5			ns	

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

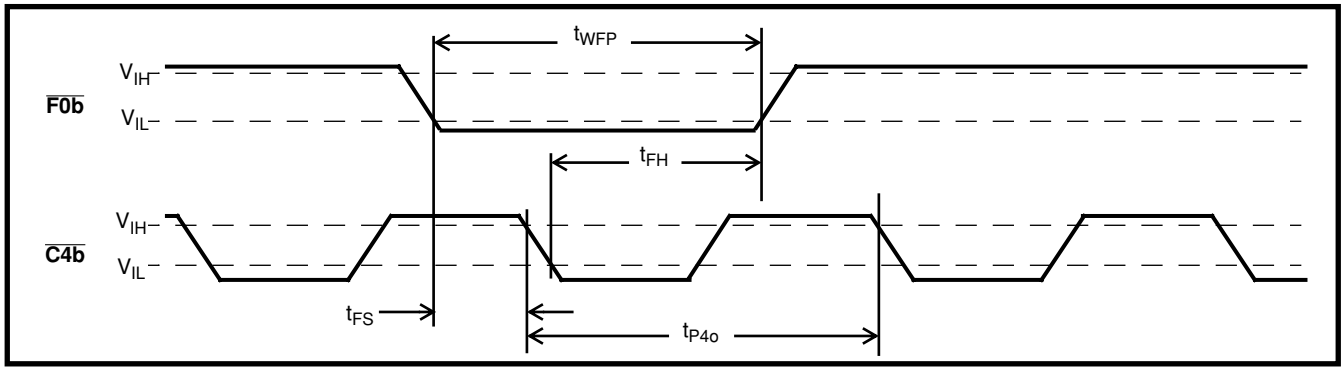


Figure 15 - External Inputs on $\overline{C4b}$ and $\overline{F0b}$ for the DPLL #2

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. **(Ref. Figure 16)**

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	OUTPUT	Delay from Enable to Output (HIGH to THREE STATE)	t_{PHZ}		15	65	ns	Test load circuit 3 (Fig.17)
2		Delay from Enable to Output (LOW to THREE STATE)	t_{PLZ}		10	55	ns	Test load circuit 3 (Fig.17)
3		Delay from Enable to Output (THREE STATE to HIGH)	t_{PZH}			40	ns	Test load circuit 3 (Fig.17)
4		Delay from Enable to Output (THREE STATE to LOW)	t_{PZL}			50	ns	Test load circuit 3 (Fig.17)

† Timing is over recommended temperature & power supply voltages
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

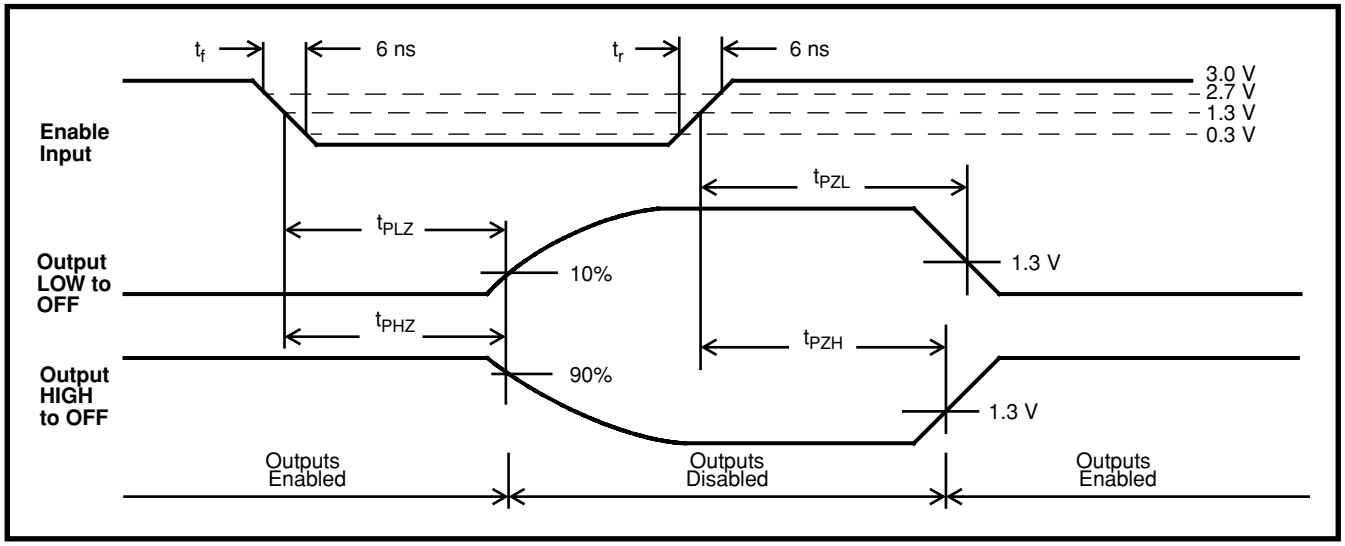


Figure 16 - Three State Outputs and Enable Timings

AC Electrical Characteristics† - Uncommitted NAND Gate

Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Propagation delay (LOW to HIGH), input Ai or Bi to output	t_{PLH}		25	40	ns	Test load circuit 1 (Fig. 17)
2	Propagation delay (HIGH to LOW), input Ai or Bi to output	t_{PHL}		20	40	ns	Test load circuit 1 (Fig. 17)

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

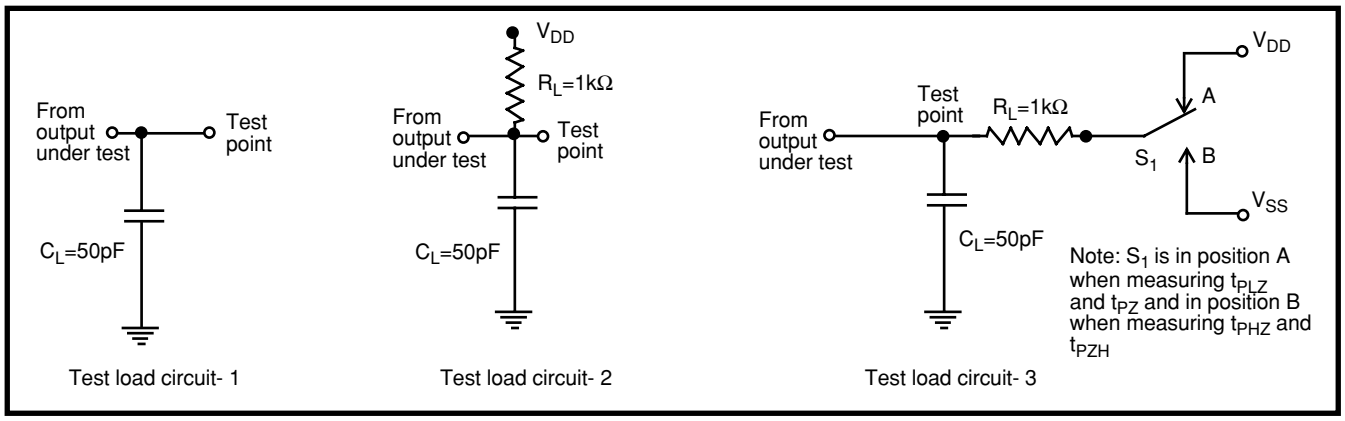
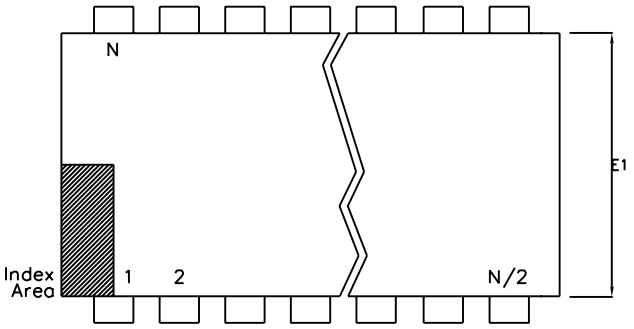
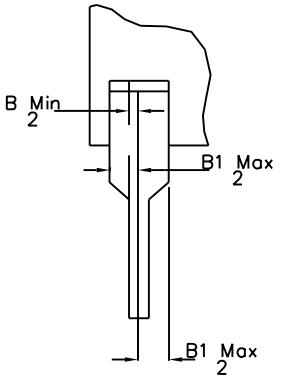
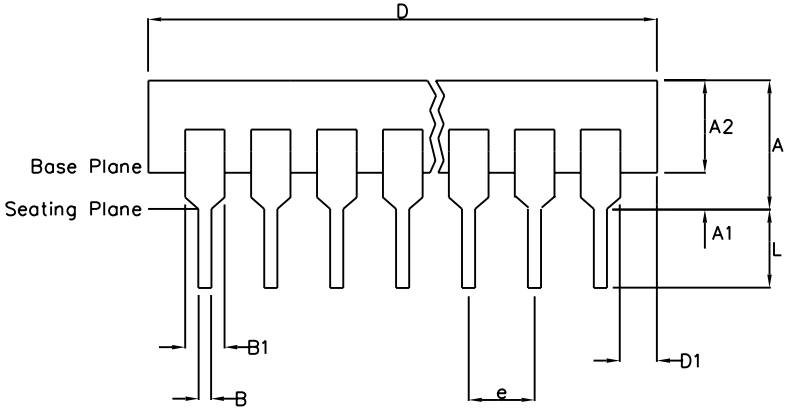
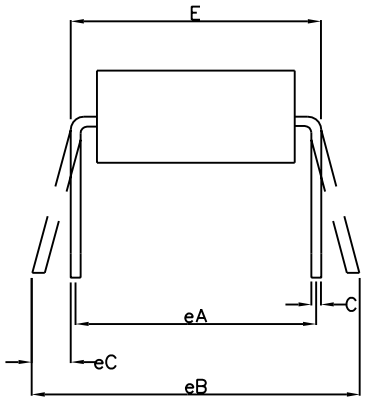


Figure 17 - Test Load Circuits









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	29.21	32.77	1.150	1.290
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	24		24	
Conforms to Jedec MS-011AA ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

ISSUE	1	2	3	
ACN	7010	203400	213101	
DATE	20Apr95	4Nov97	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

DP / E

Package Code DA

Package Outline for 24 lead PDIP

GPD00071

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