

LM611 Operational Amplifier and Adjustable Reference

Check for Samples: [LM611](#)

FEATURES

- **OP AMP**
- **Low operating current:** 300 μ A (op amp)
- **Wide supply voltage range:** 4V to 36V
- **Wide common-mode range:** V^- to ($V^+ - 1.8V$)
- **Wide differential input voltage:** $\pm 36V$
- **Available in low cost 8-pin DIP**
- **Available in plastic package rated for Military Temperature Range Operation**
- **REFERENCE**
- **Adjustable output voltage:** 1.2V to 6.3V

- **Tight initial tolerance available:** $\pm 0.6\%$
- **Wide operating current range:** 17 μ A to 20 mA
- **Reference floats above ground**
- **Tolerant of load capacitance**

APPLICATIONS

- **Transducer bridge driver**
- **Process and Mass Flow Control systems**
- **Power supply voltage monitor**
- **Buffered voltage references for A/D's**

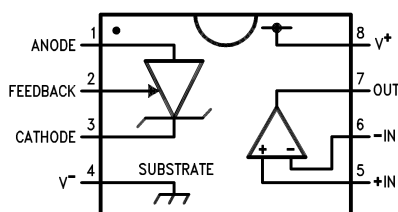
DESCRIPTION

The LM611 consists of a single-supply op-amp and a programmable voltage reference in one space saving 8-pin package. The op-amp out-performs most single-supply op-amps by providing higher speed and bandwidth along with low supply current. This device was specifically designed to lower cost and board space requirements in transducer, test, measurement and data acquisition systems.

Combining a stable voltage reference with a wide output swing op-amp makes the LM611 ideal for single supply transducers, signal conditioning and bridge driving where large common-mode signals are common. The voltage reference consists of a reliable band-gap design that maintains low dynamic output impedance (1 Ω typical), excellent initial tolerance (0.6%), and the ability to be programmed from 1.2V to 6.3V via two external resistors. The voltage reference is very stable even when driving large capacitive loads, as are commonly encountered in CMOS data acquisition systems.

As a member of National's Super-Block™ family, the LM611 is a space-saving monolithic alternative to a multi-chip solution, offering a high level of integration without sacrificing performance.

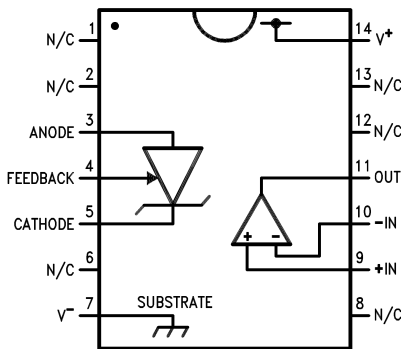
Connection Diagram



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings ⁽¹⁾

Voltage on Any Pins Except V_R	
(referred to V^- pin)	36V (Max)
⁽²⁾	-0.3V (Min)
Current through Any Input Pin and	
V_R Pin	± 20 mA
Differential Input Voltage	
Military and Industrial	± 36 V
Commercial	± 32 V
Storage Temperature Range	$-65^\circ\text{C} \leq T_J \leq +150^\circ\text{C}$
Maximum Junction Temperature	150°C
Thermal Resistance, Junction-to-Ambient ⁽³⁾	
N Package	100°C/W
M Package	150°C/W
Soldering Information Soldering (10 seconds)	
N Package	260°C
M Package	220°C
ESD Tolerance ⁽⁴⁾	± 1 kV

- (1) Absolute maximum ratings indicate limits beyond which damage to the component may occur. Electrical specifications do not apply when operating the device beyond its rated operating conditions.
- (2) More accurately, it is excessive current flow, with resulting excess heating, that limits the voltages on all pins. When any pin is pulled a diode drop below V^- , a parasitic NPN transistor turns ON. No latch-up will occur as long as the current through that pin remains below the Maximum Rating. Operation is undefined and unpredictable when any parasitic diode or transistor is conducting.
- (3) Junction temperature may be calculated using $T_J = T_A + P_D \theta_{JA}$. The given thermal resistance is worst-case for packages in sockets in still air. For packages soldered to copper-clad board with dissipation from one op amp or reference output transistor, nominal θ_{JA} is 90°C/W for the N package and 135°C/W for the M package.
- (4) Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Operating Temperature Range

LM611AI, LM611I, LM611BI	$-40^\circ\text{C} \leq T_J \leq +85^\circ\text{C}$
LM611AM, LM611M	$-55^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$
LM611C	$0^\circ\text{C} \leq T_J \leq 70^\circ\text{C}$

Electrical Characteristics

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\ \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (1)	LM611AM	LM611M	Units
				LM611AI	LM611BI	
				Limits (2)	Limits (2)	
I_{S}	Total Supply Current	$R_{\text{LOAD}} = \infty$,	210	300	350	$\mu\text{A max}$
		$4\text{V} \leq V^+ \leq 36\text{V}$ (32V for LM611C)	221	320	370	$\mu\text{A max}$
V_{S}	Supply Voltage Range		2.2	2.8	2.8	V min
			2.9	3	3	V min
			46	36	32	V max
			43	36	32	V max
OPERATIONAL AMPLIFIER						
V_{OS1}	V_{OS} Over Supply	$4\text{V} \leq V^+ \leq 36\text{V}$	1.5	3.5	5.0	mV max
		$(4\text{V} \leq V^+ \leq 32\text{V for LM611C})$	2.0	6.0	7.0	mV max
V_{OS2}	V_{OS} Over V_{CM}	$V_{\text{CM}} = 0\text{V}$ through $V_{\text{CM}} =$	1.0	3.5	5.0	mV max
		$(V^+ - 1.8\text{V}), V^+ = 30\text{V}, V^- = 0\text{V}$	1.5	6.0	7.0	mV max
$\frac{V_{\text{OS3}}}{\Delta T}$	Average V_{OS} Drift	(2)	15			$\mu\text{V}/^\circ\text{C}$
						max
I_{B}	Input Bias Current		10	25	35	nA max
			11	30	40	nA max
I_{OS}	Input Offset Current		0.2	4	4	nA max
			0.3	5	5	nA max
$\frac{I_{\text{OS1}}}{\Delta T}$	Average Offset Drift Current		4			$\text{pA}/^\circ\text{C}$
R_{IN}	Input Resistance	Differential	1800			$\text{M}\Omega$
		Common-Mode	3800			$\text{M}\Omega$
C_{IN}	Input Capacitance	Common-Mode	5.7			pF
e_{n}	Voltage Noise	$f = 100\ \text{Hz}$, Input Referred	74			$\text{nV}/\sqrt{\text{Hz}}$
I_{n}	Current Noise	$f = 100\ \text{Hz}$, Input Referred	58			$\text{fA}/\sqrt{\text{Hz}}$
CMRR	Common-Mode Rejection-Ratio	$V^+ = 30\text{V}, 0\text{V} \leq V_{\text{CM}} \leq (V^+ - 1.8\text{V})$	95	80	75	dB min
		$\text{CMRR} = 20 \log (\Delta V_{\text{CM}}/\Delta V_{\text{OS}})$	90	75	70	dB min
PSRR	Power Supply Rejection-Ratio	$4\text{V} \leq V^+ \leq 30\text{V}, V_{\text{CM}} = V^+/2$,	110	80	75	dB min
		$\text{PSRR} = 20 \log (\Delta V^+/\Delta V_{\text{OS}})$	100	75	70	dB min
A_{V}	Open Loop Voltage Gain	$R_{\text{L}} = 10\ \text{k}\Omega$ to GND, $V^+ = 30\text{V}$,	500	100	94	V/mV
		$5\text{V} \leq V_{\text{OUT}} \leq 25\text{V}$	50	40	40	min
SR	Slew Rate	$V^+ = 30\text{V}$ (3)	0.70	0.55	0.50	V/ μs
			0.65	0.45	0.45	
GBW	Gain Bandwidth	$C_{\text{L}} = 50\ \text{pF}$	0.80			MHz

(1) Typical values in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; values in **boldface type** apply for the full operating temperature range. These values represent the most likely parametric norm.

(2) All limits are guaranteed at room temperature (standard type face) or at operating temperature extremes (**bold face type**).

(3) Slew rate is measured with op amp in a voltage follower configuration. For rising slew rate, the input voltage is driven from 5V to 25V, and the output voltage transition is sampled at 10V and 20V. For falling slew rate, the input voltage is driven from 25V to 5V, and output voltage transition is sampled at 20V and 10V.

Electrical Characteristics (continued)

These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\ \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (1)	LM611AM	LM611BI	Units
				LM611AI	LM611I	
				(2)	Limits	
					(2)	
			0.50			
V_{O1}	Output Voltage	$R_{\text{L}} = 10\ \text{k}\Omega$ to GND	$V^+ - 1.4$	$V^+ - 1.7$	$V^+ - 1.8$	V min
	Swing High	$V^+ = 36\text{V}$ (32V for LM611C)	$V^+ - 1.6$	$V^+ - 1.9$	$V^+ - 1.9$	V min
V_{O2}	Output Voltage	$R_{\text{L}} = 10\ \text{k}\Omega$ to V^+	$V^- + 0.8$	$V^- + 0.9$	$V^- + 0.95$	V max
	Swing Low	$V^+ = 36\text{V}$ (32V for LM611C)	$V^- + 0.9$	$V^- + 1.0$	$V^- + 1.0$	V max
I_{OUT}	Output Source	$V_{\text{OUT}} = 2.5\text{V}$, $V_{+\text{IN}} = 0\text{V}$,	25	20	16	mA min
	Current	$V_{-\text{IN}} = -0.3\text{V}$	15	13	13	mA min
I_{SINK}	Output Sink	$V_{\text{OUT}} = 1.6\text{V}$, $V_{+\text{IN}} = 0\text{V}$,	17	14	13	mA min
	Current	$V_{-\text{IN}} = 0.3\text{V}$	9	8	8	mA min
I_{SHORT}	Short Circuit Current	$V_{\text{OUT}} = 0\text{V}$, $V_{+\text{IN}} = 3\text{V}$,	30	50	50	mA max
		$V_{-\text{IN}} = 2\text{V}$, Source	40	60	60	mA max
		$V_{\text{OUT}} = 5\text{V}$, $V_{+\text{IN}} = 2\text{V}$,	30	60	70	mA max
		$V_{-\text{IN}} = 3\text{V}$, Sink	32	80	90	mA max
VOLTAGE REFERENCE						
V_{R}	Reference Voltage	(4)	1.244	1.2365	1.2191	V min
				1.2515	1.2689	V max
				($\pm 0.6\%$)	($\pm 2.0\%$)	
$\frac{\Delta V_{\text{R}}}{\Delta T_{\text{J}}}$	Average Temperature Drift	(5)	10	80	150	PPM/ $^\circ\text{C}$ max
$\frac{\Delta V_{\text{R}}}{\Delta T_{\text{J}}}$	Hysteresis	Hyst = $(V_{\text{R}'} - V_{\text{R}0})/\Delta T_{\text{J}}$ (6)	3.2			$\mu\text{V}/^\circ\text{C}$
$\frac{\Delta V_{\text{R}}}{\Delta I_{\text{R}}}$	V_{R} Change	$V_{\text{R}(100\ \mu\text{A})} - V_{\text{R}(17\ \mu\text{A})}$	0.05	1	1	mV max
	with Current		0.1	1.1	1.1	mV max
		$V_{\text{R}(10\ \text{mA})} - V_{\text{R}(100\ \mu\text{A})}$ (7)	1.5	5	5	mV max
			2.0	5.5	5.5	mV max
R	Resistance	$\Delta V_{\text{R}(10 \rightarrow 0.1\ \text{mA})}/9.9\ \text{mA}$	0.2	0.56	0.56	Ω max
		$\Delta V_{\text{R}(100 \rightarrow 17\ \mu\text{A})}/83\ \mu\text{A}$	0.6	13	13	Ω max
$\frac{\Delta V_{\text{R}}}{V_{\text{RO}}}$	V_{R} Change with	$V_{\text{R}(V_{\text{RO}} = V_{\text{I}})} - V_{\text{R}(V_{\text{RO}} = 6.3\text{V})}$	2.5	7	7	mV max
	High V_{RO}	(5.06V between Anode and FEEDBACK)	2.8	10	10	mV max

(4) V_{R} is the cathode-feedback voltage, nominally 1.244V.

(5) Average reference drift is calculated from the measurement of the reference voltage at 25°C and at the temperature extremes. The drift, in ppm/ $^\circ\text{C}$, is $10^6 \cdot \Delta V_{\text{R}} / (V_{\text{R}[25^\circ\text{C}]} \cdot \Delta T_{\text{J}})$, where ΔV_{R} is the lowest value subtracted from the highest, $V_{\text{R}[25^\circ\text{C}]}$ is the value at 25°C , and ΔT_{J} is the temperature range. This parameter is guaranteed by design and sample testing.

(6) Hysteresis is the change in V_{R} caused by a change in T_{J} , after the reference has been "dehysteresized". To dehysteresize the reference; that is minimize the hysteresis to the typical value, its junction temperature should be cycled in the following pattern, spiraling in toward 25°C : 25°C , 85°C , -40°C , 70°C , 0°C , 25°C .

(7) Low contact resistance is required for accurate measurement.

Electrical Characteristics (continued)

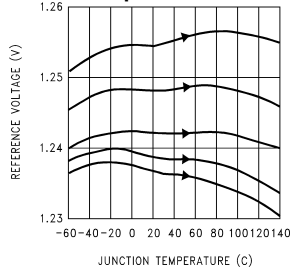
These specifications apply for $V^- = \text{GND} = 0\text{V}$, $V^+ = 5\text{V}$, $V_{\text{CM}} = V_{\text{OUT}} = 2.5\text{V}$, $I_{\text{R}} = 100\ \mu\text{A}$, FEEDBACK pin shorted to GND, unless otherwise specified. Limits in standard typeface are for $T_{\text{J}} = 25^\circ\text{C}$; limits in **boldface type** apply over the **Operating Temperature Range**.

Symbol	Parameter	Conditions	Typical (1)	LM611M		Units
				LM611AM	LM611BI	
				LM611AI	LM611I	
				(2)	Limits	
				(2)	Limits	
				(2)	Limits	
$\frac{\Delta V_{\text{R}}}{\Delta V^+}$	V_{R} Change with	$V_{\text{R}(V^+ = 5\text{V})} - V_{\text{R}(V^+ = 3.6\text{V})}$	0.1	1.2	1.2	mV max
	V^+ Change	($V^+ = 32\text{V}$ for LM611C)	0.1	1.3	1.3	mV max
		$V_{\text{R}(V^+ = 5\text{V})} - V_{\text{R}(V^+ = 3\text{V})}$	0.01	1	1	mV max
			0.01	1.5	1.5	mV max
$\frac{\Delta V_{\text{R}}}{\Delta V_{\text{ANODE}}}$	V_{R} Change with	$V^+ = V^+ \text{ max, } \Delta V_{\text{R}} = V_{\text{R}}$				
	V_{ANODE} Change	(@ $V_{\text{ANODE}} = V^- = \text{GND}$) - V_{R} (@ $V_{\text{ANODE}} = V^+ - 1.0\text{V}$)	0.7 3.3	1.5 3.0	1.6 3.0	mV max mV max
I_{FB}	FEEDBACK Bias	I_{FB} ; $V_{\text{ANODE}} \leq V_{\text{FB}} \leq 5.06\text{V}$	22	35	50	nA max
	Current		29	40	55	nA max
ϵ_{n}	V_{R} Noise	10 Hz to 10,000 Hz, $V_{\text{RO}} = V_{\text{R}}$	30			μV_{RMS}

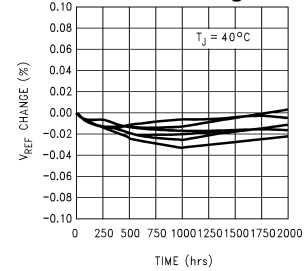
Typical Performance Characteristics (Reference)

$T_J = 25^\circ\text{C}$, FEEDBACK pin shorted to $V^- = 0\text{V}$, unless otherwise noted

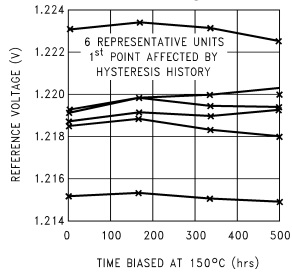
Reference Voltage vs Temp
on 5 Representative Units



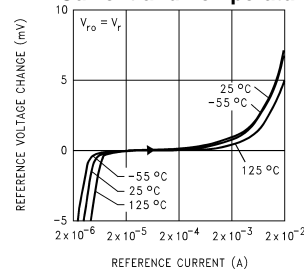
Reference Voltage Drift



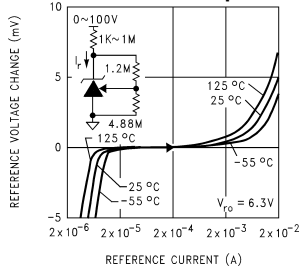
Accelerated Reference Voltage Drift vs Time



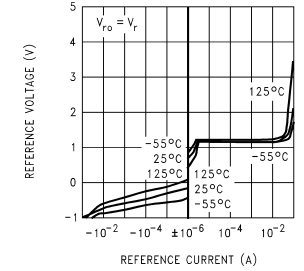
Reference Voltage vs Current and Temperature



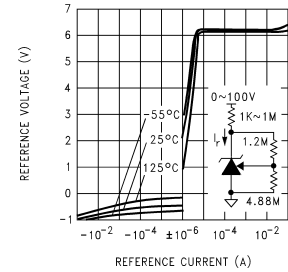
Reference Voltage vs Current and Temperature



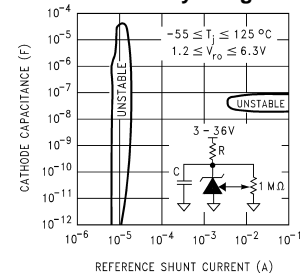
Reference Voltage vs Reference Current



Reference Voltage vs Reference Current

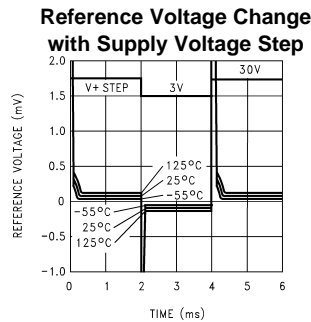
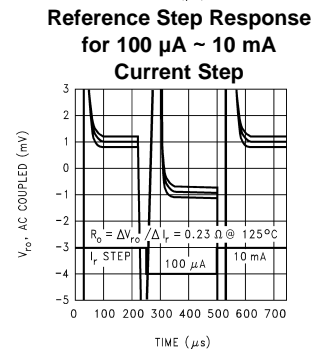
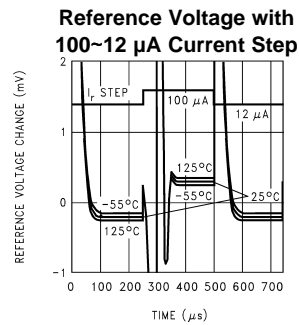
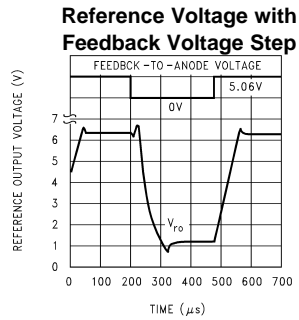
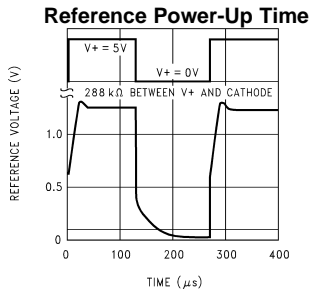
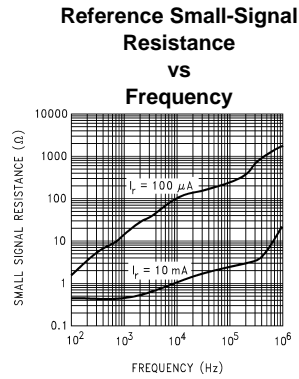
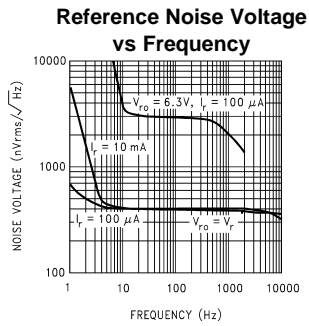
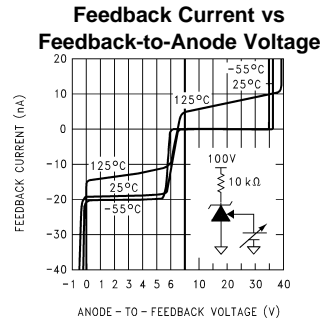
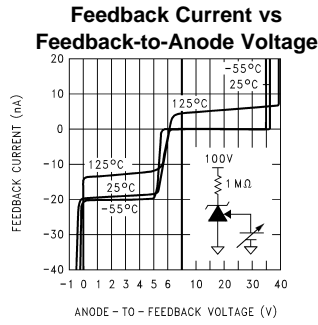


Reference AC Stability Range



Typical Performance Characteristics (Reference) (continued)

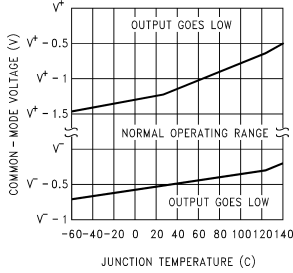
T_J = 25°C, FEEDBACK pin shorted to V⁻ = 0V, unless otherwise noted



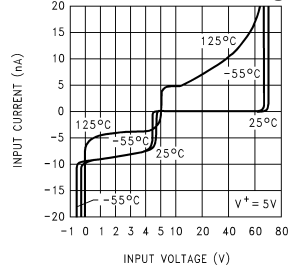
Typical Performance Characteristics (Op Amps)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

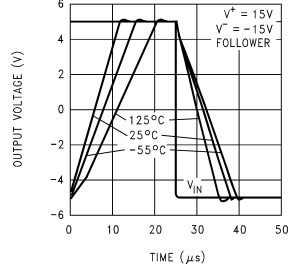
Input Common-Mode Voltage Range vs Temperature



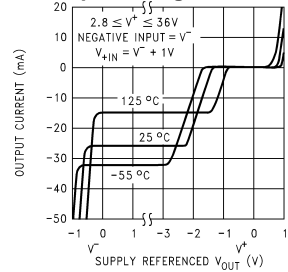
Input Bias Current vs Common-Mode Voltage



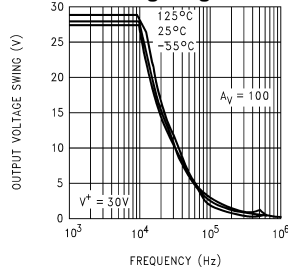
Large-Signal Step Response



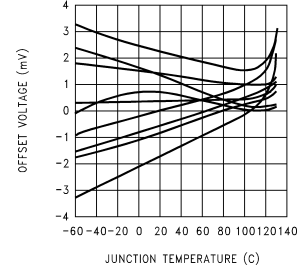
Output Source Current vs Output Voltage and Temp.



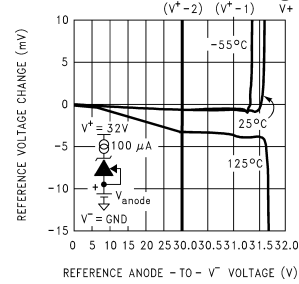
Output Swing, Large Signal



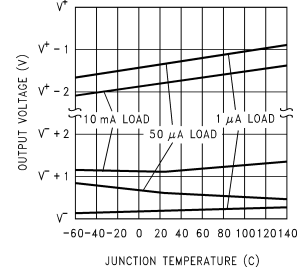
Vos vs Junction Temperature



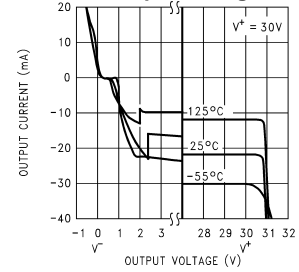
Reference Change vs Common-Mode Voltage



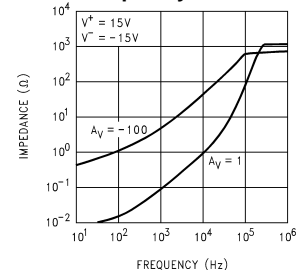
Output Voltage Swing vs Temp. and Current



Output Sink Current vs Output Voltage



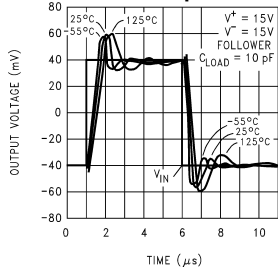
Output Impedance vs Frequency and Gain



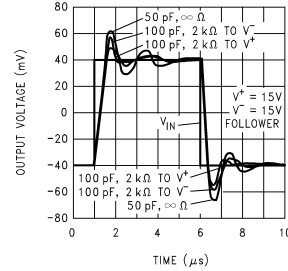
Typical Performance Characteristics (Op Amps) (continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

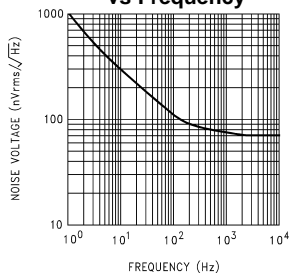
Small Signal Pulse Response vs Temp.



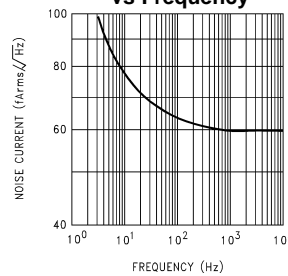
Small-Signal Pulse Response vs Load



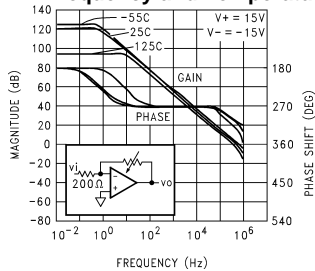
Op Amp Voltage Noise vs Frequency



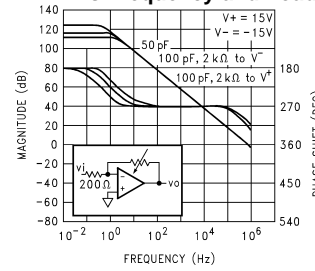
Op Amp Current Noise vs Frequency



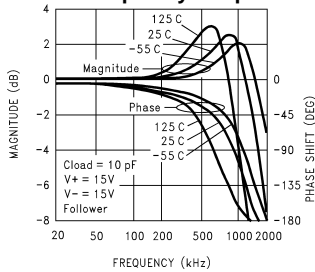
Small-Signal Voltage Gain vs Frequency and Temperature



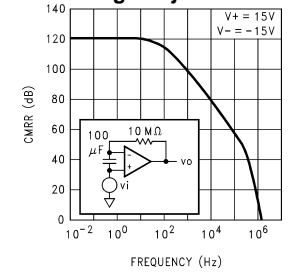
Small-Signal Voltage Gain vs Frequency and Load



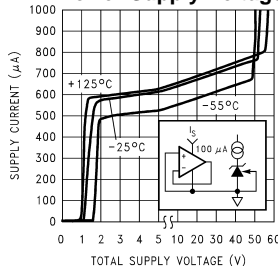
Follower Small-Signal Frequency Response



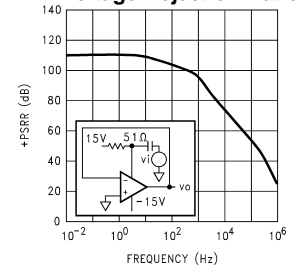
Common-Mode Input Voltage Rejection Ratio



Power Supply Current vs Power Supply Voltage



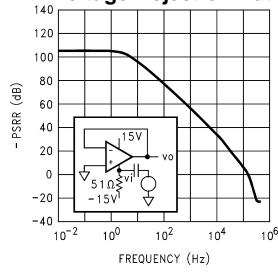
Positive Power Supply Voltage Rejection Ratio



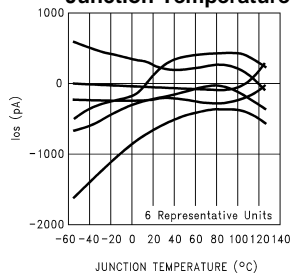
Typical Performance Characteristics (Op Amps) (continued)

$V^+ = 5V$, $V^- = GND = 0V$, $V_{CM} = V^+/2$, $V_{OUT} = V^+/2$, $T_J = 25^\circ C$, unless otherwise noted

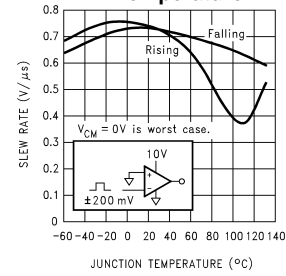
Negative Power Supply Voltage Rejection Ratio



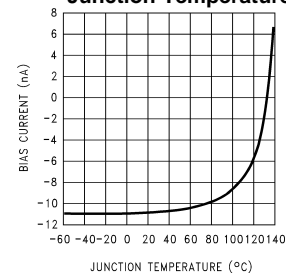
Input Offset Current vs Junction Temperature



Slew Rate vs Temperature

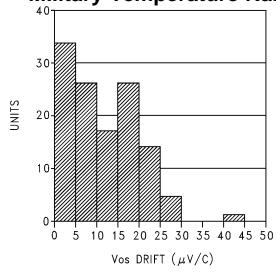


Input Bias Current vs Junction Temperature

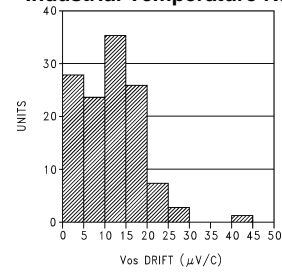


Typical Performance Distributions

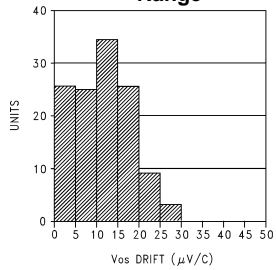
**Average V_{OS} Drift
Military Temperature Range**



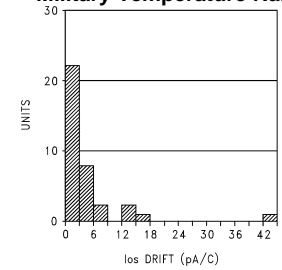
**Average V_{OS} Drift
Industrial Temperature Range**



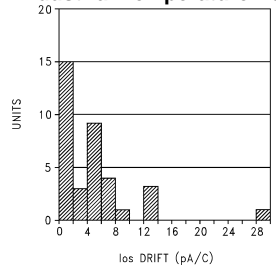
**Average V_{OS} Drift
Commercial Temperature Range**



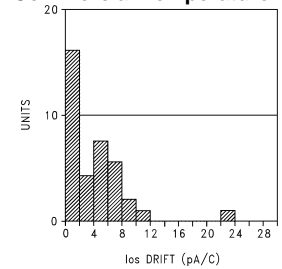
**Average I_{OS} Drift
Military Temperature Range**



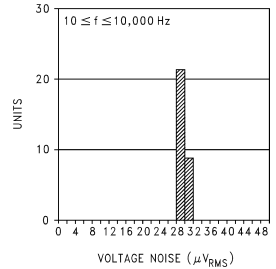
**Average I_{OS} Drift
Industrial Temperature Range**



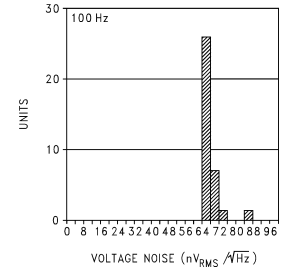
**Average I_{OS} Drift
Commercial Temperature Range**



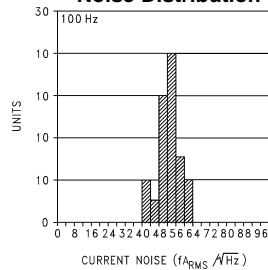
**Voltage Reference Broad-Band
Noise Distribution**



**Op Amp Voltage
Noise Distribution**



**Op Amp Current
Noise Distribution**

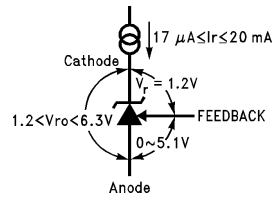


Application Information

VOLTAGE REFERENCE

Reference Biasing

The voltage reference is of a shunt regulator topology that models as a simple zener diode. With current I_r flowing in the 'forward' direction there is the familiar diode transfer function. I_r flowing in the reverse direction forces the reference voltage to be developed from cathode to anode. The applied voltage to the cathode may range from a diode drop below V^- to the reference voltage or to the avalanche voltage of the parallel protection diode, nominally 7V. A 6.3V reference with $V^+ = 3V$ is allowed.



**Figure 1. Voltages Associated with Reference
(Current Source I_r is External)**

The reference equivalent circuit reveals how V_r is held at the constant 1.2V by feedback, and how the FEEDBACK pin passes little current.

To generate the required reverse current, typically a resistor is connected from a supply voltage higher than the reference voltage. Varying that voltage, and so varying I_r , has small effect with the equivalent series resistance of less than an ohm at the higher currents. Alternatively, an active current source, such as the LM134 series, may generate I_r .

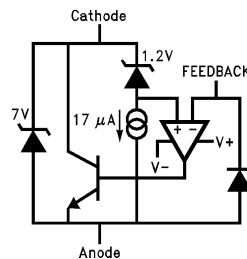


Figure 2. Reference Equivalent Circuit

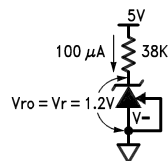


Figure 3. 1.2V Reference

Capacitors in parallel with the reference are allowed. See the Reference AC Stability Range curve for capacitance values—from 20 μ A to 3 mA any capacitor value is stable. With the reference's wide stability range with resistive and capacitive loads, a wide range of RC filter values will perform noise filtering.

Adjustable Reference

The FEEDBACK pin allows the reference output voltage, V_{ro} , to vary from 1.24V to 6.3V. The reference attempts to hold V_r at 1.24V. If V_r is above 1.24V, the reference will conduct current from Cathode to Anode; FEEDBACK current always remains low. If FEEDBACK is connected to Anode, then $V_{ro} = V_r = 1.24V$. For higher voltages FEEDBACK is held at a constant voltage above Anode—say 3.76V for $V_{ro} = 5V$. Connecting a resistor across the constant V_r generates a current $I=R1/V_r$ flowing from Cathode into FEEDBACK node. A Thevenin equivalent 3.76V is generated from FEEDBACK to Anode with $R2=3.76/I$. Keep I greater than one thousand times larger than FEEDBACK bias current for <0.1% error— $I \geq 32 \mu A$ for the military grade over the military temperature range ($I \geq 5.5 \mu A$ for a 1% untrimmed error for a commercial part.)

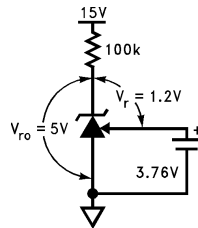
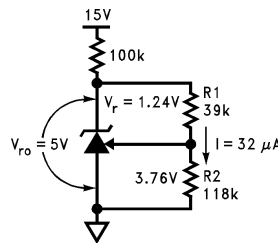


Figure 4. Thevenin Equivalent of Reference with 5V Output



$$R1 = Vr/I = 1.24/32\mu = 39k$$

$$R2 = R1 \{(Vro/Vr) - 1\} = 39k \{(5/1.24) - 1\} = 118k$$

Figure 5. Resistors R1 and R2 Program Reference Output Voltage to be 5V

Understanding that V_r is fixed and that voltage sources, resistors, and capacitors may be tied to the FEEDBACK pin, a range of V_r temperature coefficients may be synthesized.

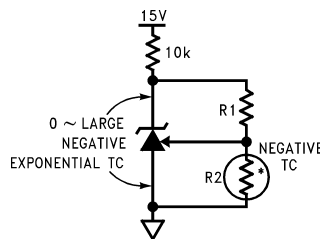


Figure 6. Output Voltage has Negative Temperature Coefficient (TC) if R2 has Negative TC

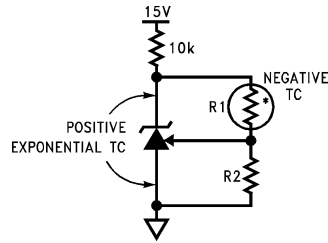


Figure 7. Output Voltage has Positive TC if R1 has Negative TC

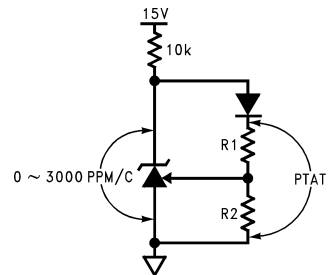
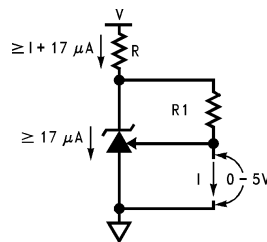


Figure 8. Diode in Series with R1 Causes Voltage Across R1 and R2 to be Proportional to Absolute Temperature (PTAT)

Connecting a resistor across Cathode-to-FEEDBACK creates a 0 TC current source, but a range of TCs may be synthesized.



$$I = Vr/R1 = 1.24/R1$$

Figure 9. Current Source is Programmed by R1

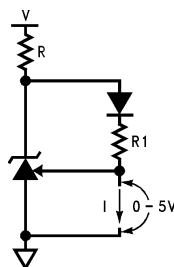


Figure 10. Proportional-to-Absolute-Temperature Current Source

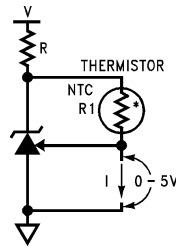


Figure 11. Negative -TC Current Source

Hysteresis

The reference voltage depends, slightly, on the thermal history of the die. Competitive micro-power products vary—always check the data sheet for any given device. Do not assume that no specification means no hysteresis.

OPERATIONAL AMPLIFIER

The amp or the reference may be biased in any way with no effect on the other, except when a substrate diode conducts (see Guaranteed Electrical Characteristics Note 1). The amp may have inputs outside the common-mode range, may be operated as a comparator, or have all terminals floating with no effect on the reference (tying inverting input to output and non-inverting input to V^- on unused amp is preferred). Choosing operating points that cause oscillation, such as driving too large a capacitive load, is best avoided.

Op Amp Output Stage

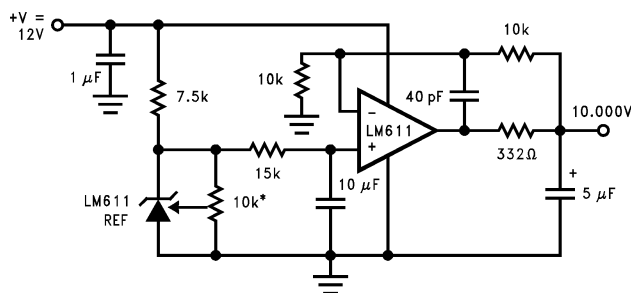
The op amp, like the LM124 series, has a flexible and relatively wide-swing output stage. There are simple rules to optimize output swing, reduce cross-over distortion, and optimize capacitive drive capability:

1. Output Swing: Unloaded, the 42 μA pull-down will bring the output within 300 mV of V^- over the military temperature range. If more than 42 μA is required, a resistor from output to V^- will help. Swing across any load may be improved slightly if the load can be tied to V^+ , at the cost of poorer sinking open-loop voltage gain.
2. Cross-over Distortion: The LM611 has lower cross-over distortion (a 1 V_{BE} deadband versus 3 V_{BE} for the LM124), and increased slew rate as shown in the characteristic curves. A resistor pull-up or pull-down will force class-A operation with only the PNP or NPN output transistor conducting, eliminating cross-over distortion.
3. Capacitive Drive: Limited by the output pole caused by the output resistance driving capacitive loads, a pull-down resistor conducting 1 mA or more reduces the output stage NPN r_e until the output resistance is that of the current limit 25 Ω . 200 pF may then be driven without oscillation.

Op Amp Input Stage

The lateral PNP input transistors, unlike those of most op amps, have BV_{EBO} equal to the absolute maximum supply voltage. Also, they have no diode clamps to the positive supply nor across the inputs. These features make the inputs look like high impedances to input sources producing large differential and common-mode voltages.

Typical Applications



*10k must be low
t.c. trim pot.

Figure 12. Ultra Low Noise 10.00V Reference.
Total Output Noise is Typically $14 \mu\text{V}_{\text{RMS}}$.
Adjust the 10k pot for 10.000V.

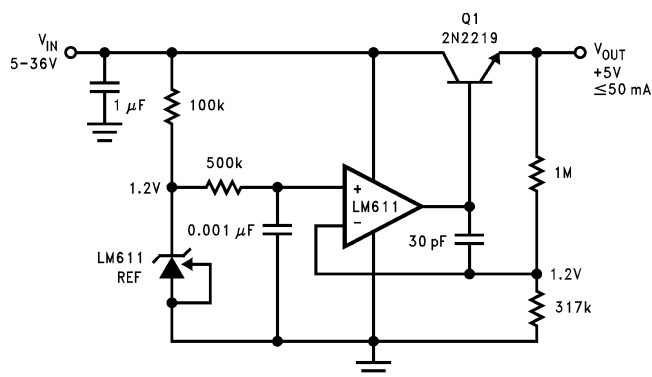
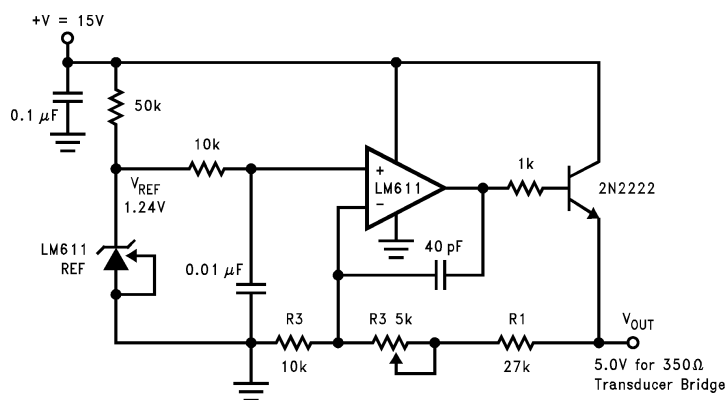


Figure 13. Simple Low Quiescent Drain Voltage Regulator. Total Supply Current is approximately $320 \mu\text{A}$ when $V_{\text{IN}} = 5\text{V}$, and output has no load.



$V_{\text{OUT}} = (R1/R2 + 1) V_{\text{REF}}$.
R1, R2 should be 1% metal film.
R3 should be low t.c. trim pot.

**Figure 14. Slow Rise-Time Upon Power-Up,
Adjustable Transducer Bridge Driver.**
Rise-time is approximately 0.5 ms.

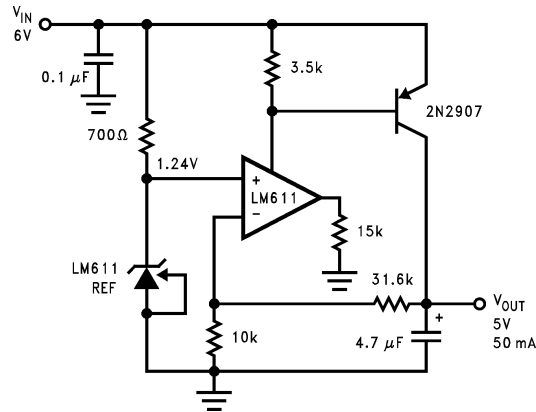


Figure 15. Low Drop-Out Voltage Regulator Circuit. Drop out voltage is typically 0.2V.

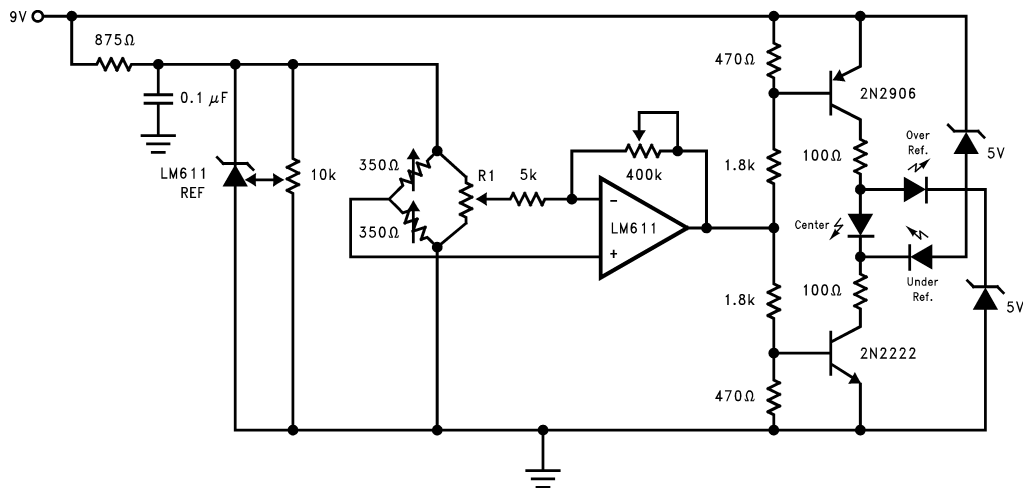


Figure 16. Nulling Bridge Detection System. Adjust sensitivity via 400 kΩ pot. Null offset with R1, and bridge drive with the 10k pot.

Simplified Schematic Diagrams

Figure 17. Op Amp

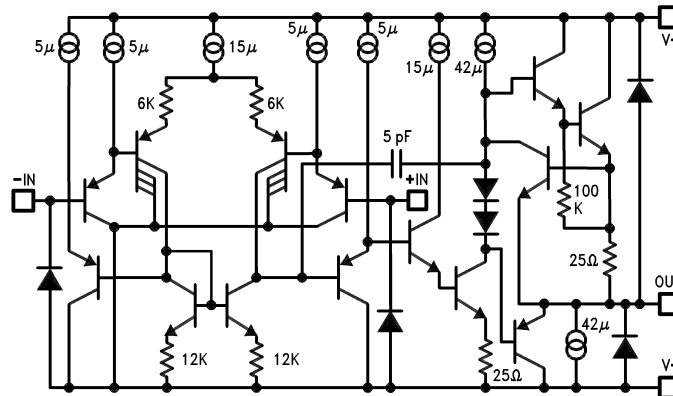


Figure 18. Reference

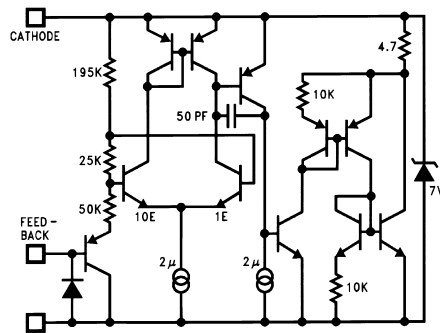
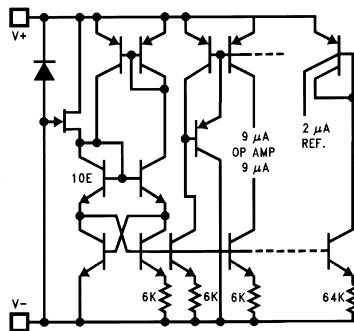


Figure 19. Bias



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM611CM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	0 to 70	LM611CM	Samples
LM611CM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM611CM	Samples
LM611CMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	0 to 70	LM611CM	Samples
LM611CMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM611CM	Samples
LM611IM	ACTIVE	SOIC	D	14	55	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM611IM	Samples
LM611IM/NOPB	ACTIVE	SOIC	D	14	55	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM611IM	Samples
LM611IMX	ACTIVE	SOIC	D	14	2500	TBD	CU SNPB	Level-1-235C-UNLIM	-40 to 85	LM611IM	Samples
LM611IMX/NOPB	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 85	LM611IM	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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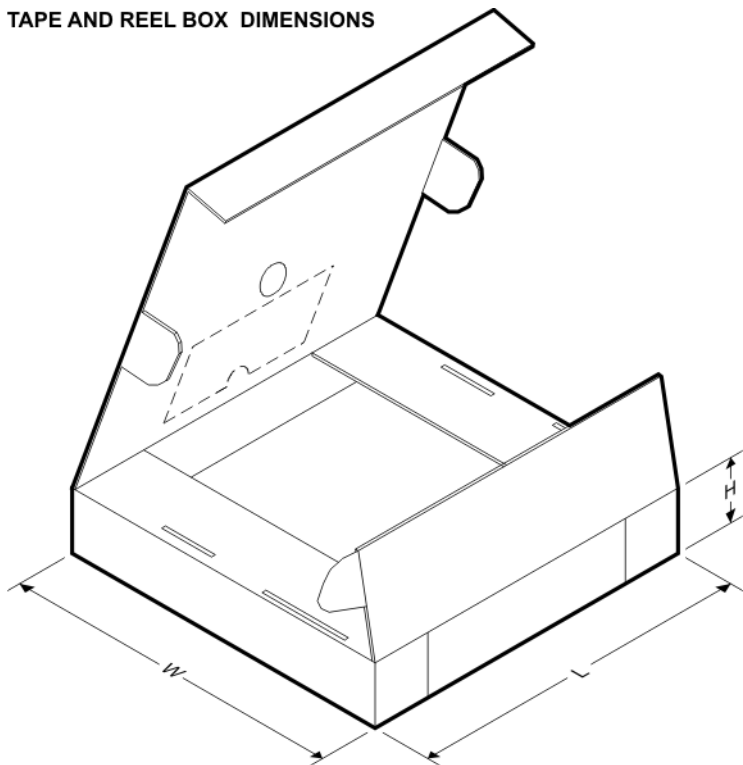
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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM611CMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM611CMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM611IMX	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1
LM611IMX/NOPB	SOIC	D	14	2500	330.0	16.4	6.5	9.35	2.3	8.0	16.0	Q1

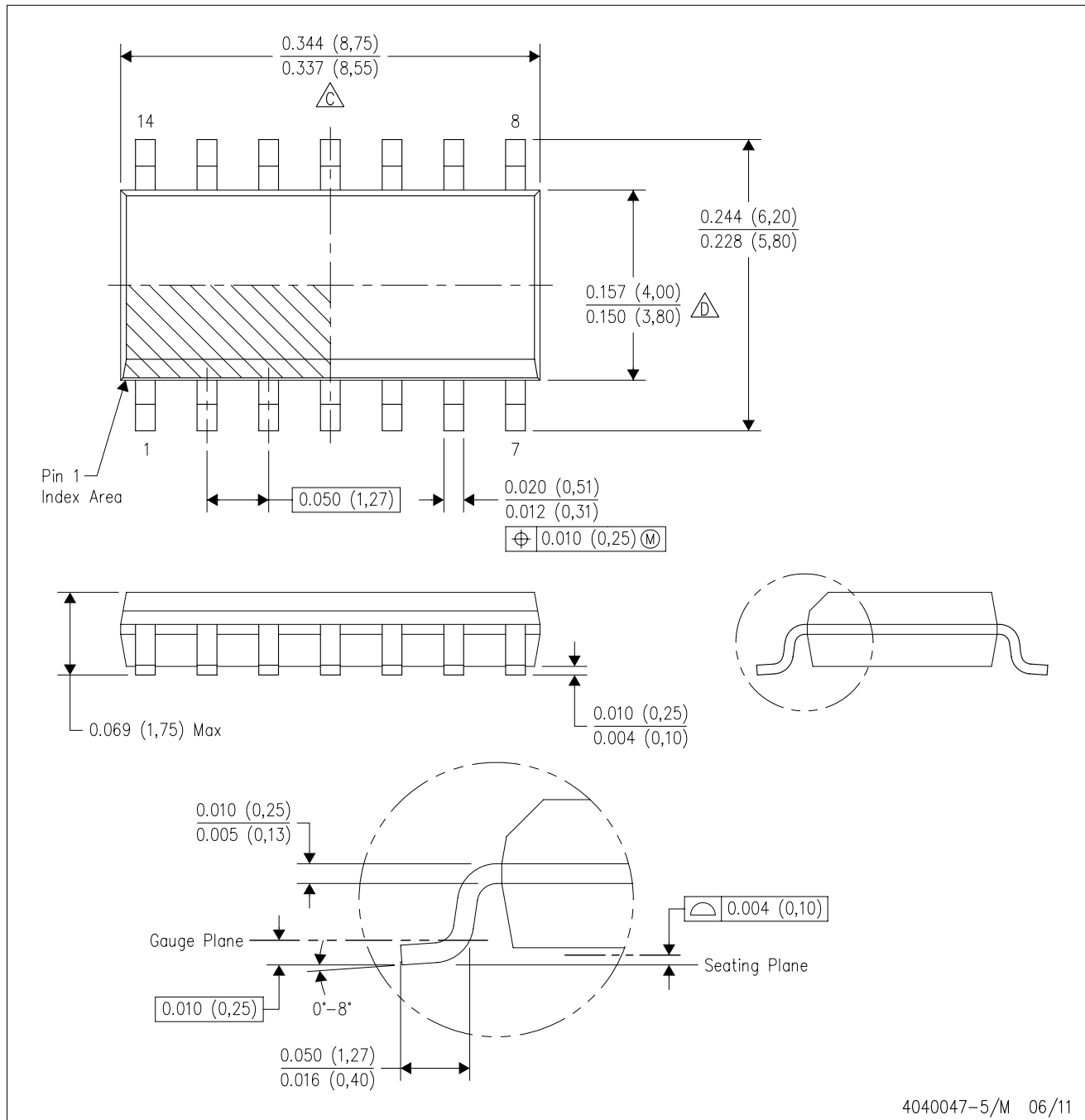
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM611CMX	SOIC	D	14	2500	349.0	337.0	45.0
LM611CMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0
LM611IMX	SOIC	D	14	2500	349.0	337.0	45.0
LM611IMX/NOPB	SOIC	D	14	2500	349.0	337.0	45.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AB.

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